FIG.1A PRIOR ART

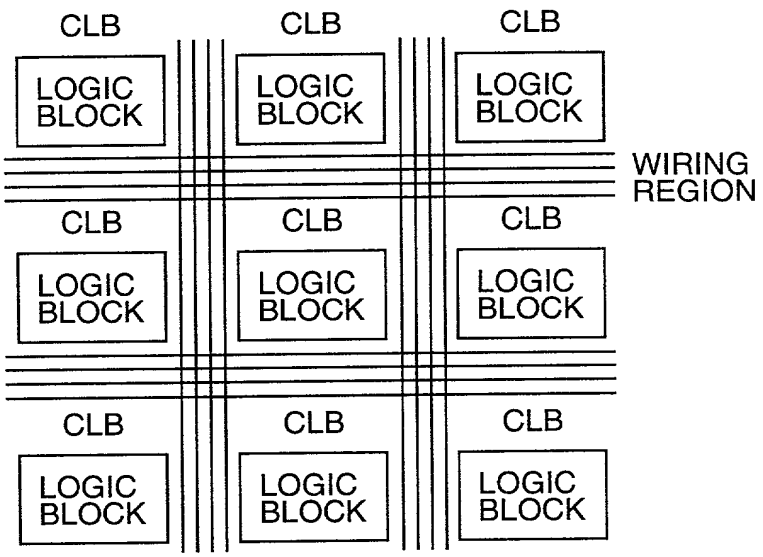


FIG.1B PRIOR ART

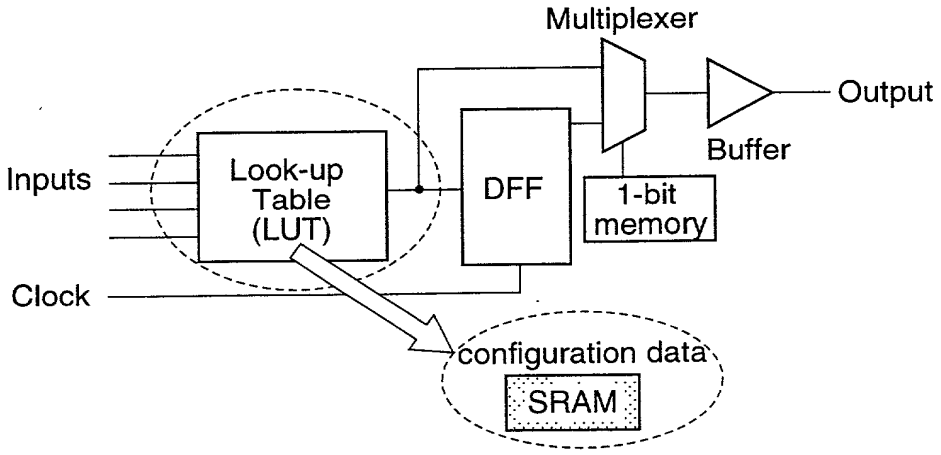


FIG.2A PRIOR ART

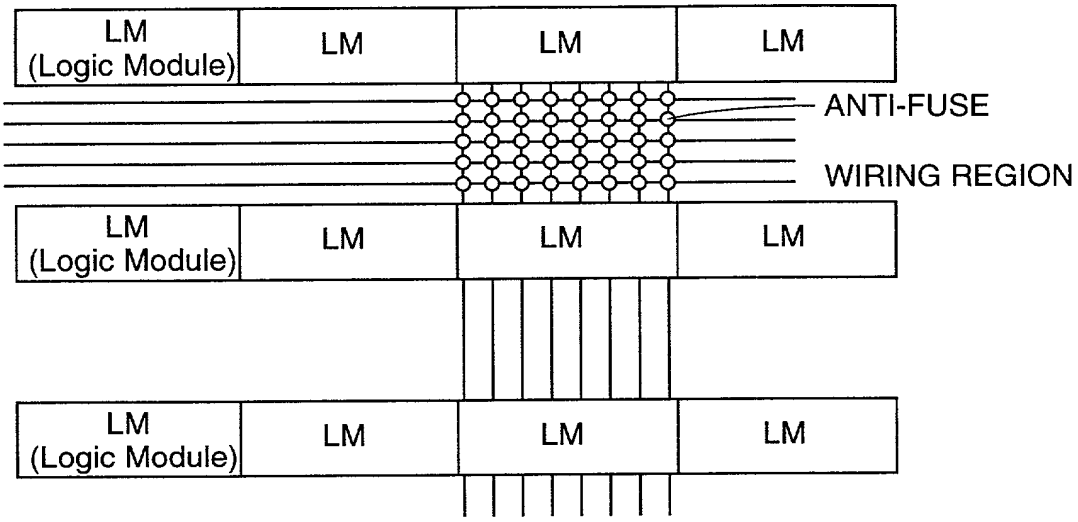


FIG.2B PRIOR ART

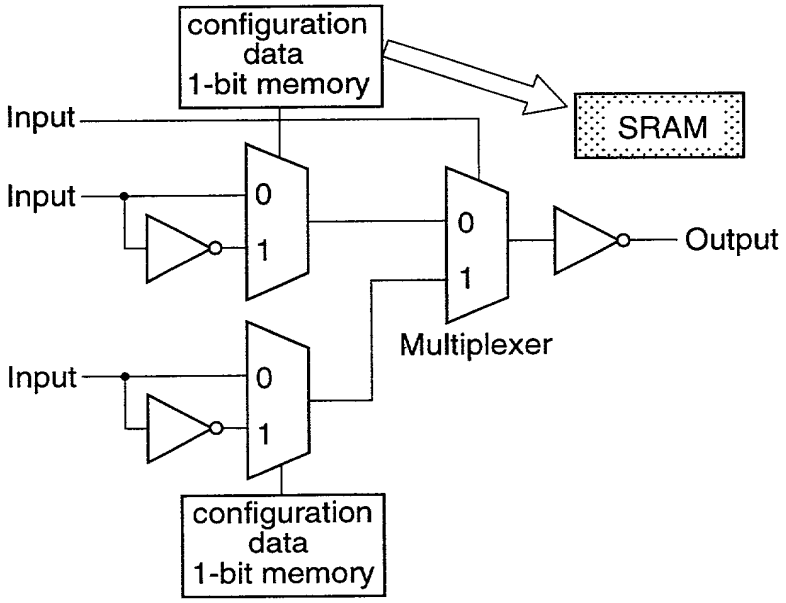


FIG.3 PRIOR ART

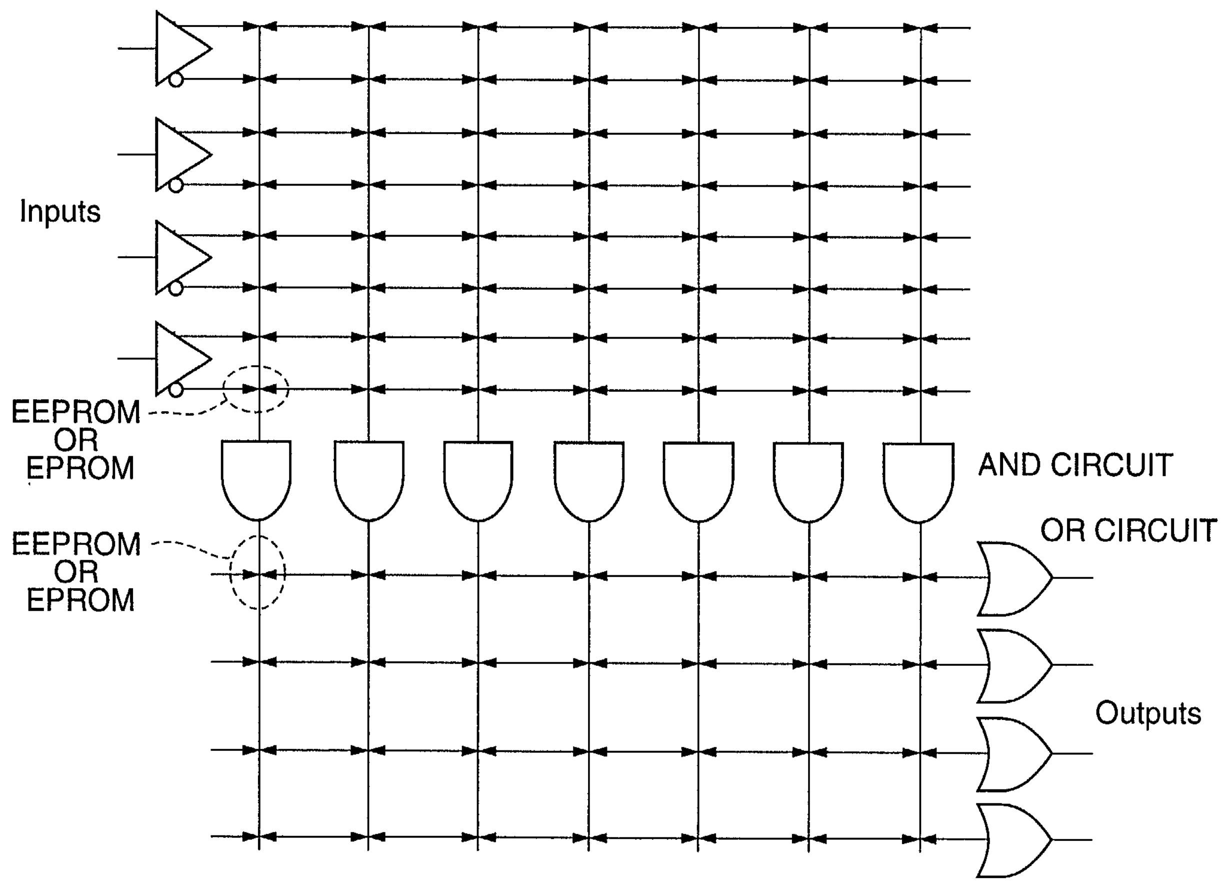


FIG.4 PRIOR ART

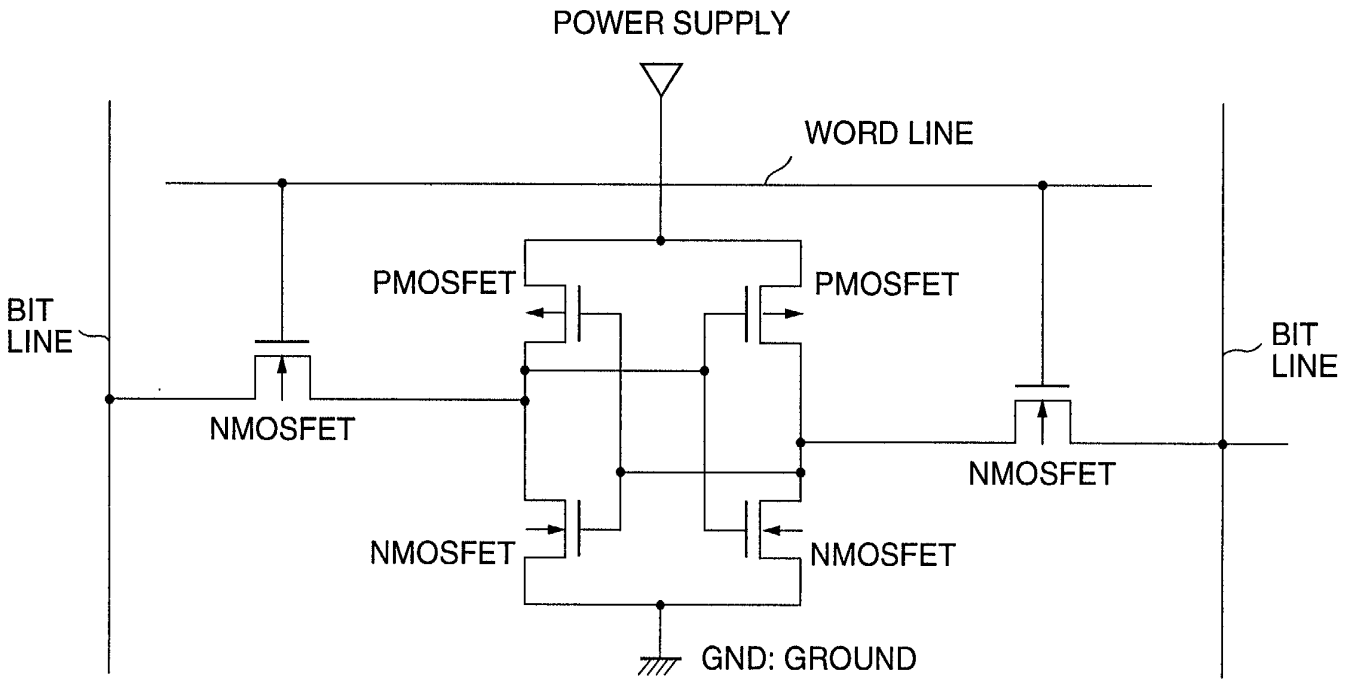


FIG.5A PRIOR ART

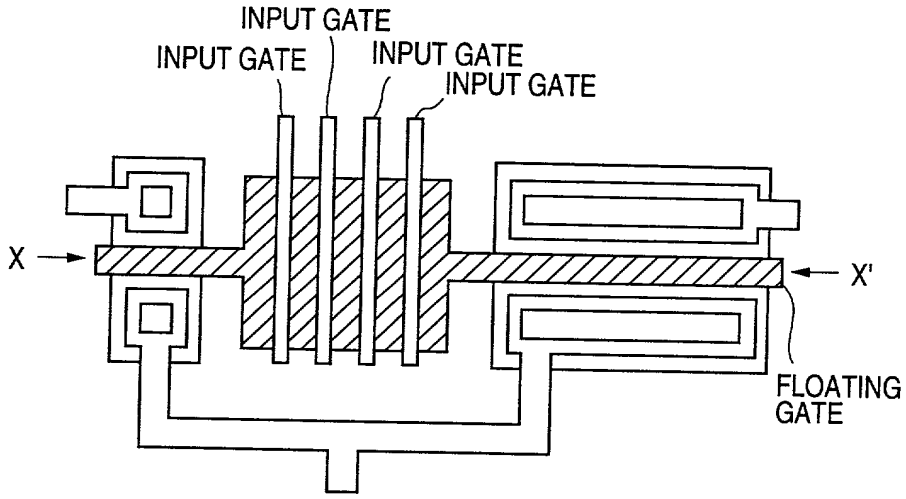


FIG.5B PRIOR ART

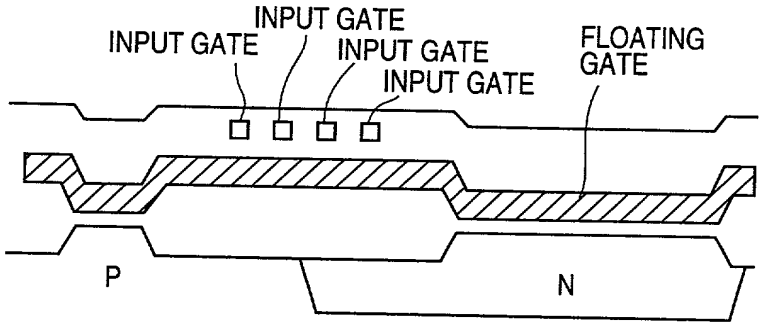


FIG.5C PRIOR ART

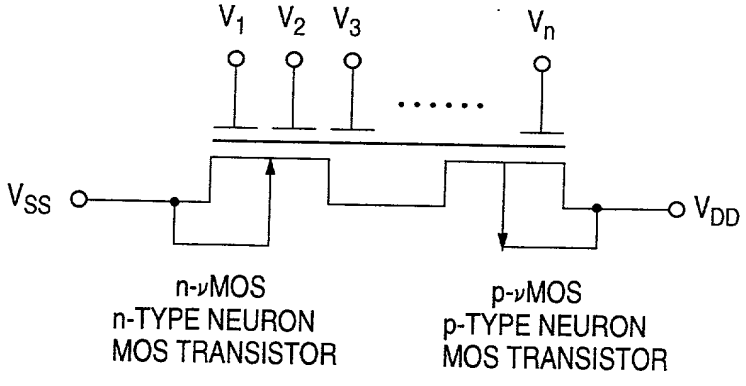


FIG.6A PRIOR ART

NEURON MOS INVERTER

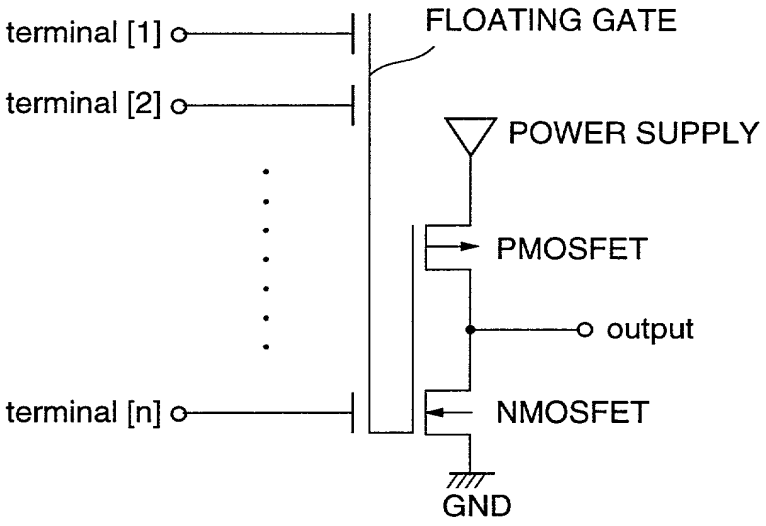


FIG.6B PRIOR ART

NEURON MOS INVERTER

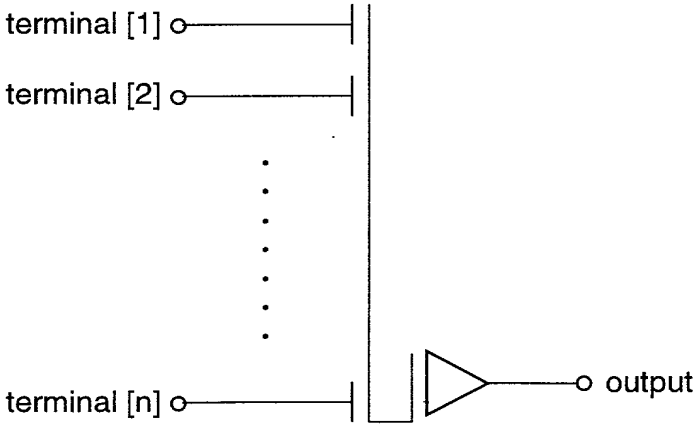


FIG.7

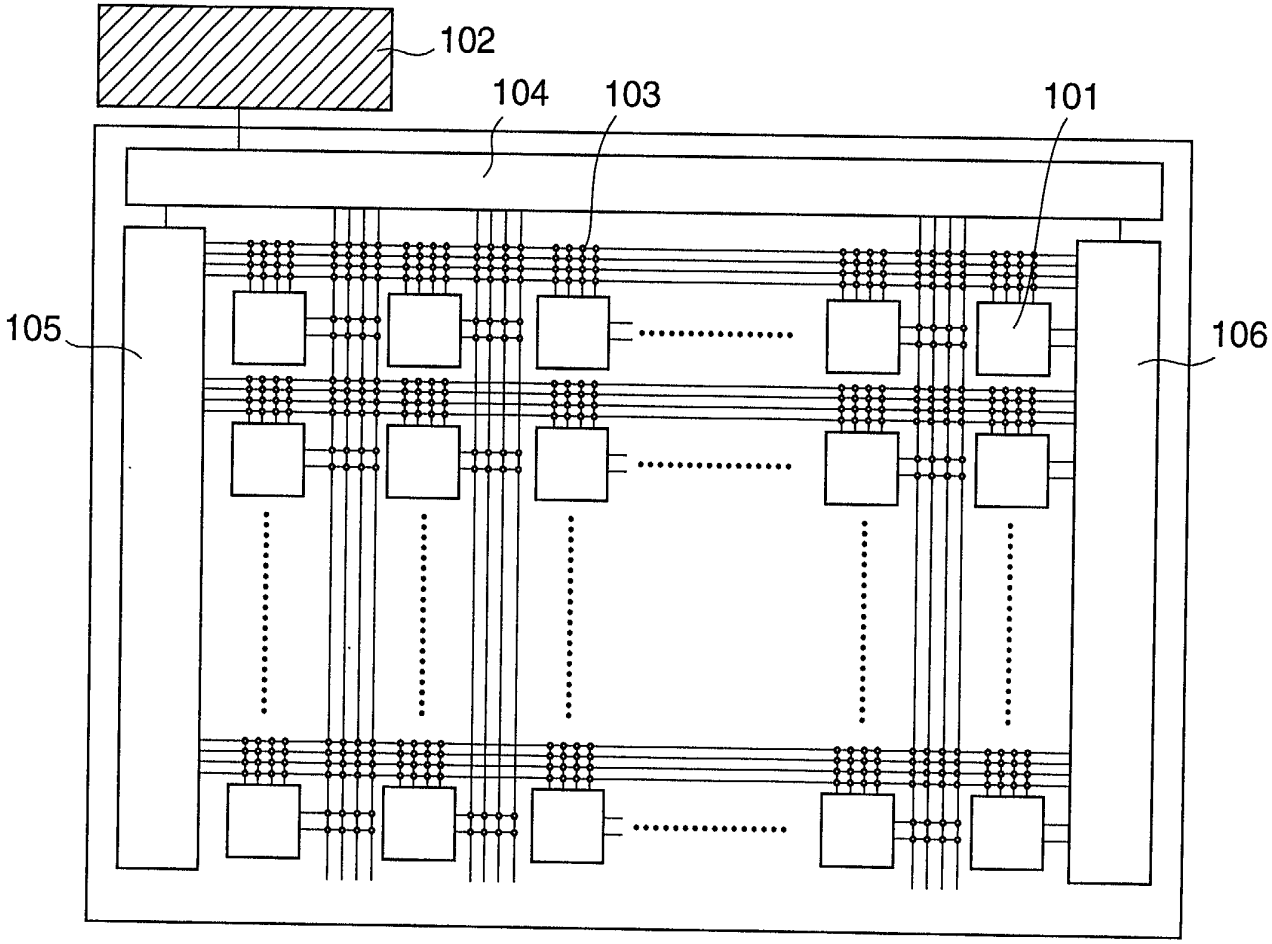


FIG.8

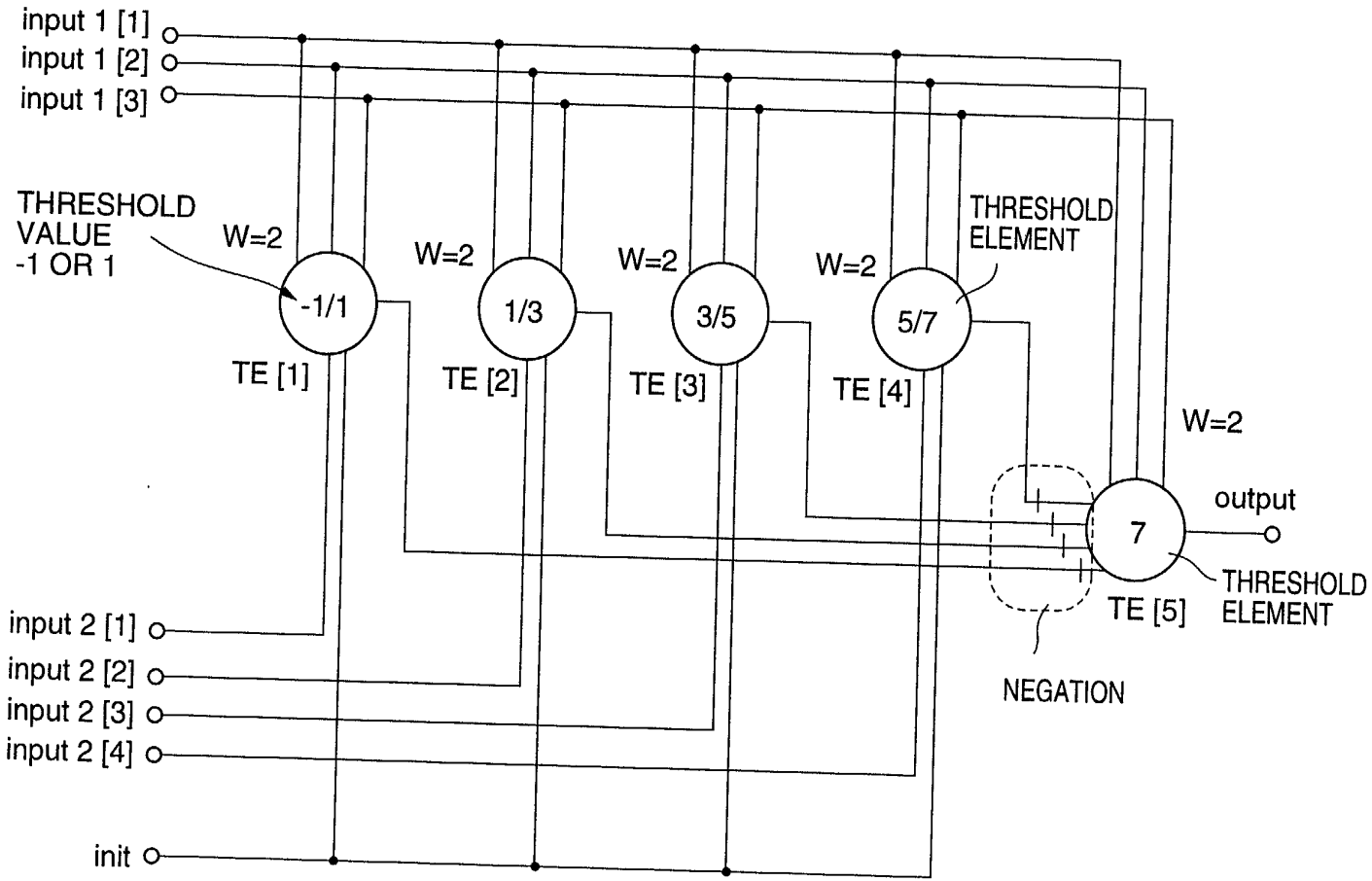


FIG.9

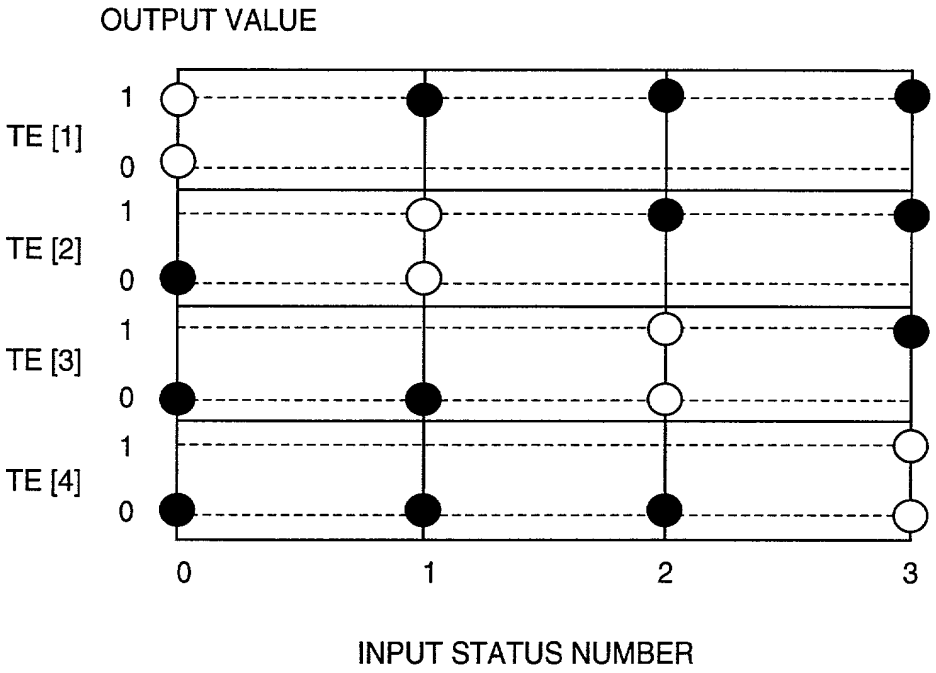

OUTPUT VALUE
TE [1]
TE [2]
TE [3]
TE [4]
1
0
1
0
1
0
1
0
0
1
2
3
INPUT STATUS NUMBER

FIG.10A

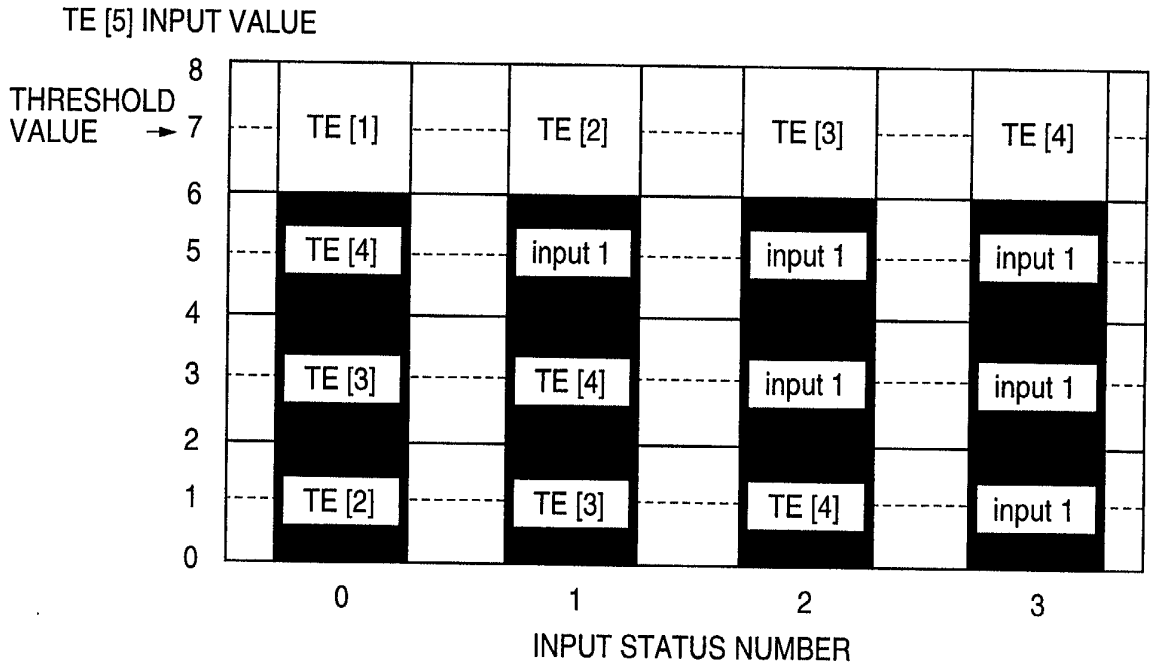


FIG.10B

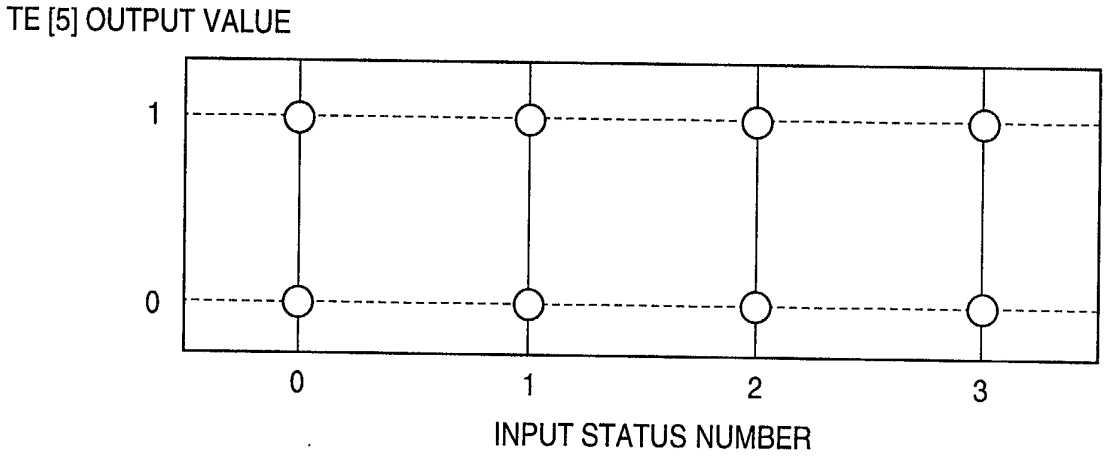


FIG.11

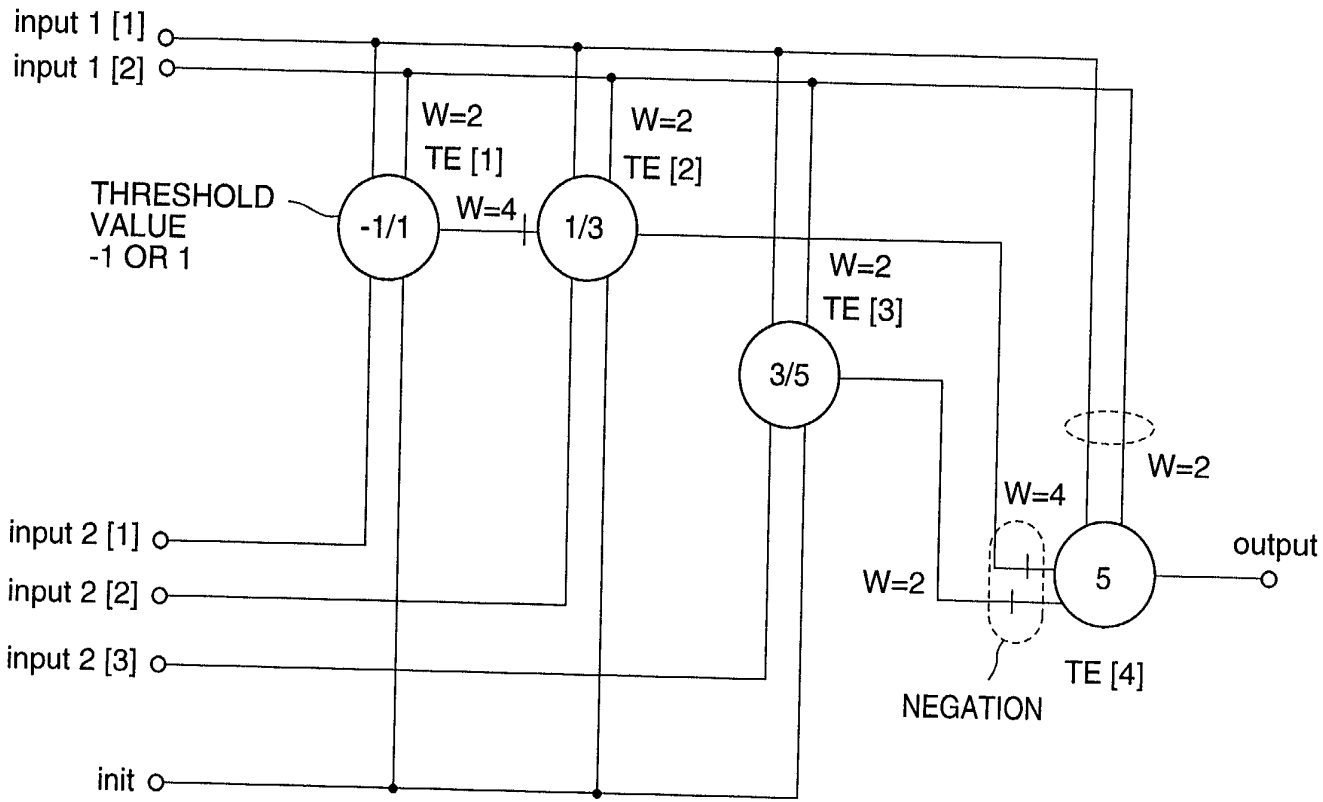


FIG.12

THRESHOLD ELEMENT	THRESHOLD VALUE	OUTPUT VALUE OF THRESHOLD ELEMENT			
		INPUT STATUS NUMBER			
		0		1	2
TE [1]	-1	1		1	1
	1	0			
TE [2]	1	OUTPUT VALUE OF TE [1]=1	0	1	1
		OUTPUT VALUE OF TE [0]=0	1		
	3	OUTPUT VALUE OF TE [1]=1	0	0	
		OUTPUT VALUE OF TE [0]=0	1		
TE [3]	3	0		0	1
	5				0

FIG.13

INPUT STATUS NUMBER	0	1	2
NEGATION OF OUTPUT VALUE OF TE [2]	1	0	0
	0	1	
NEGATION OF OUTPUT VALUE OF TE [3]	1	1	0
			1
OUTPUT VALUE OF TE [4]	1	0	0
	0	1	1

FIG.14

INPUT STATUS NUMBER	0		1		2	
VALUE OF input 2 [1] TERMINAL	0	1	—	—	—	—
VALUE OF input 2 [2] TERMINAL	—	—	0	1	—	—
VALUE OF input 2 [3] TERMINAL	—	—	—	—	0	1
output TERMINAL	0	1	1	0	1	0

FIG.15

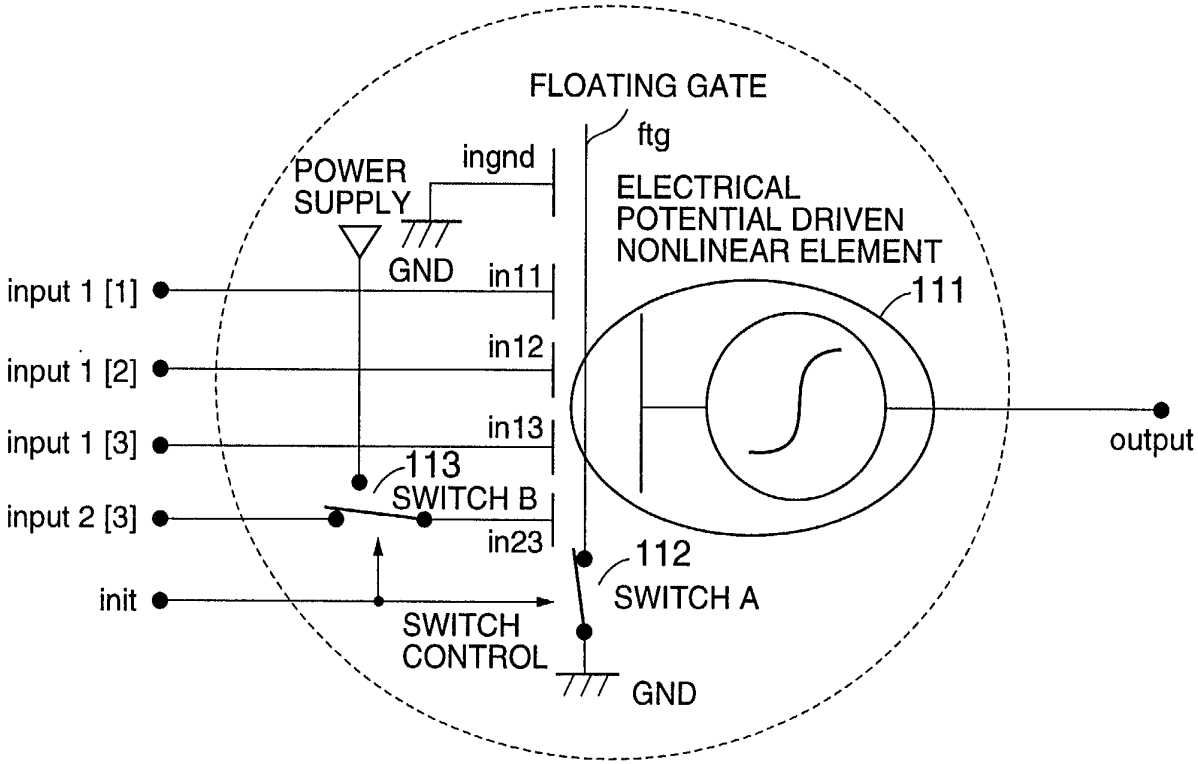


FIG.16

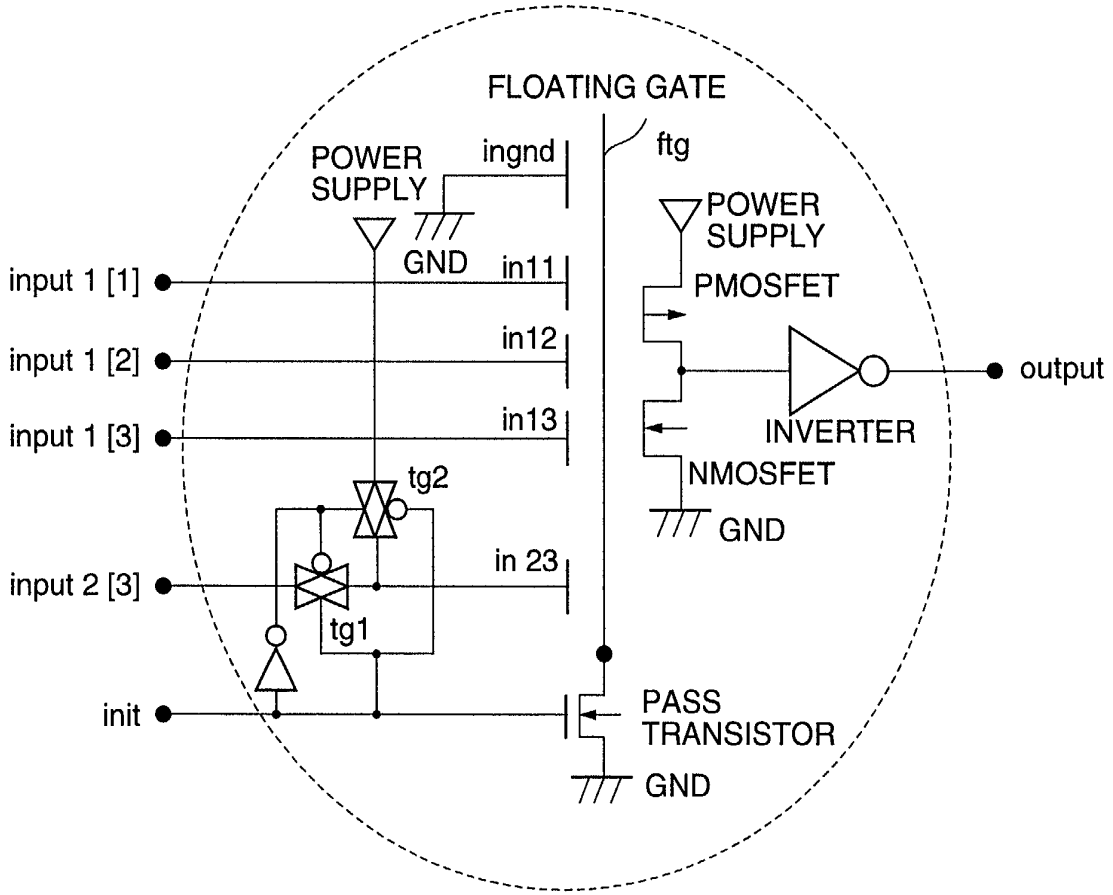


FIG.17

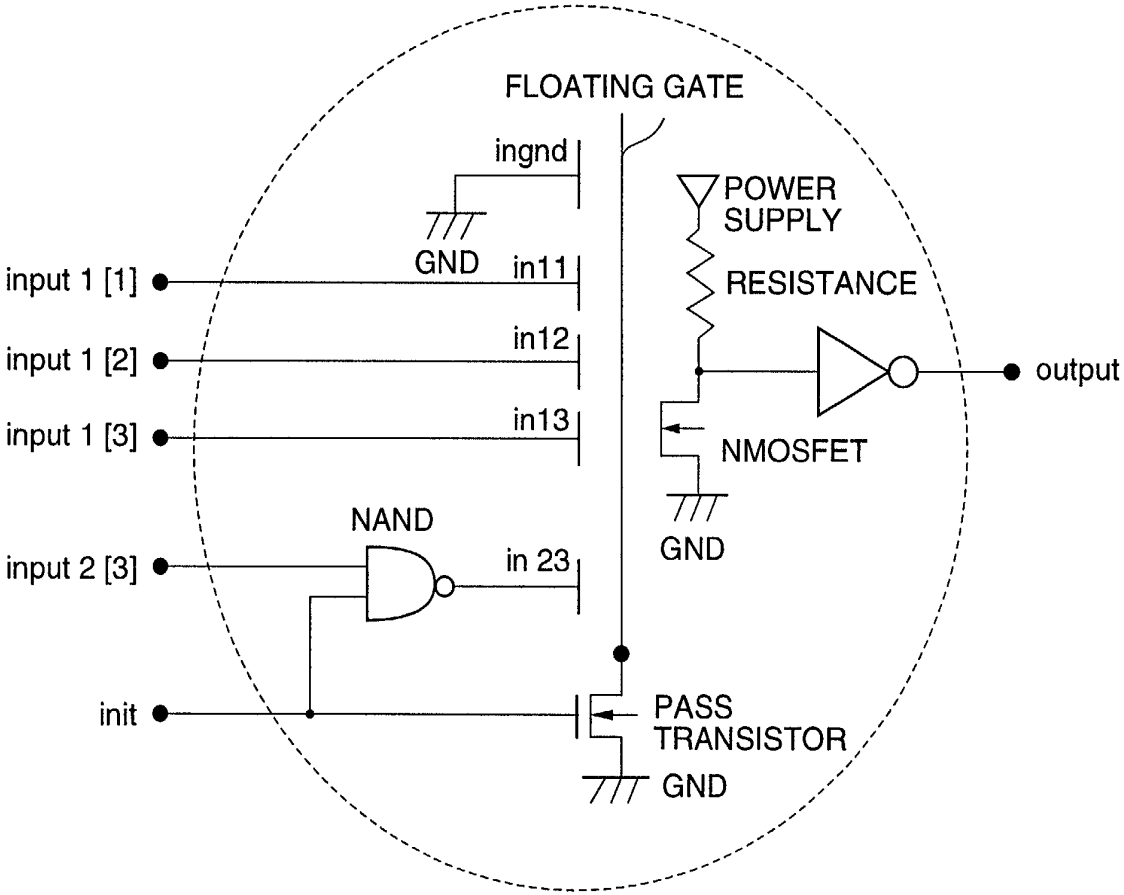

FLOATING GATE
ingnd
GND
in11
input 1 [1]
in12
input 1 [2]
in13
input 1 [3]
NAND
input 2 [3]
in 23
init
POWER SUPPLY
RESISTANCE
output
NMOSFET
GND
PASS TRANSISTOR
GND

FIG.18

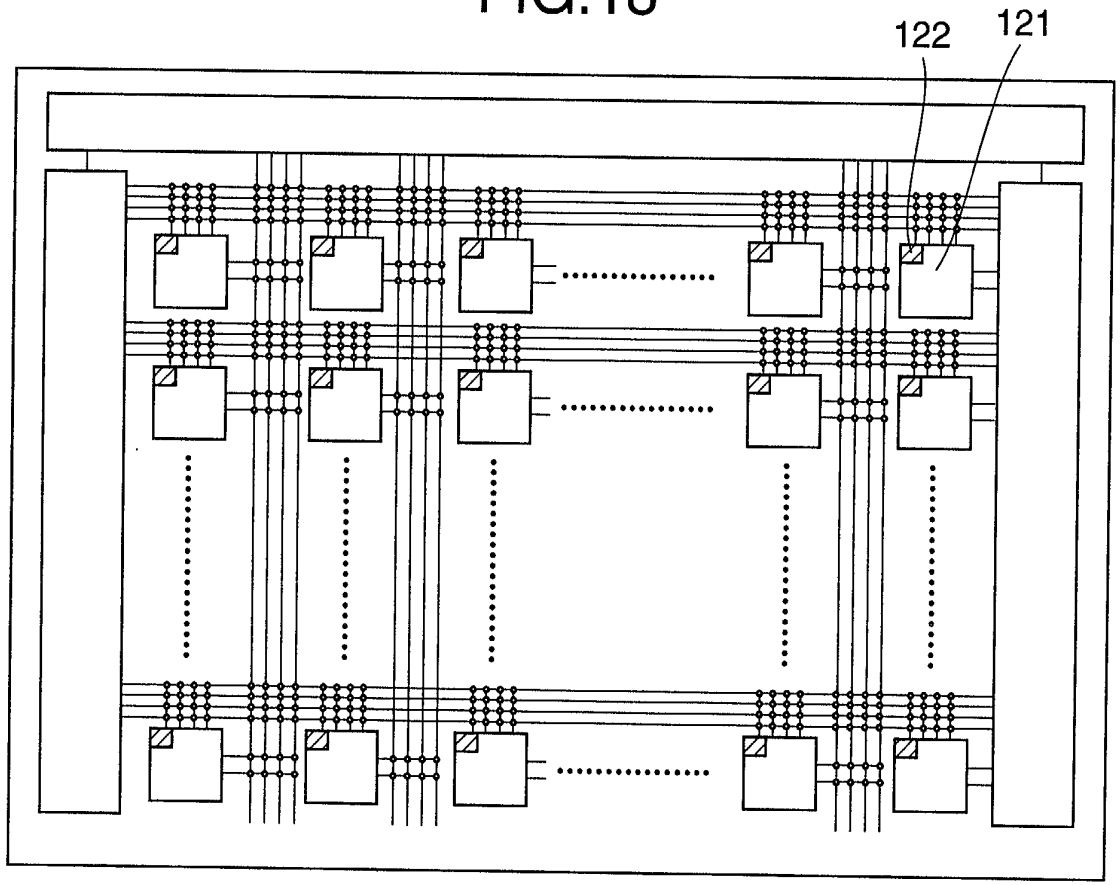


FIG19

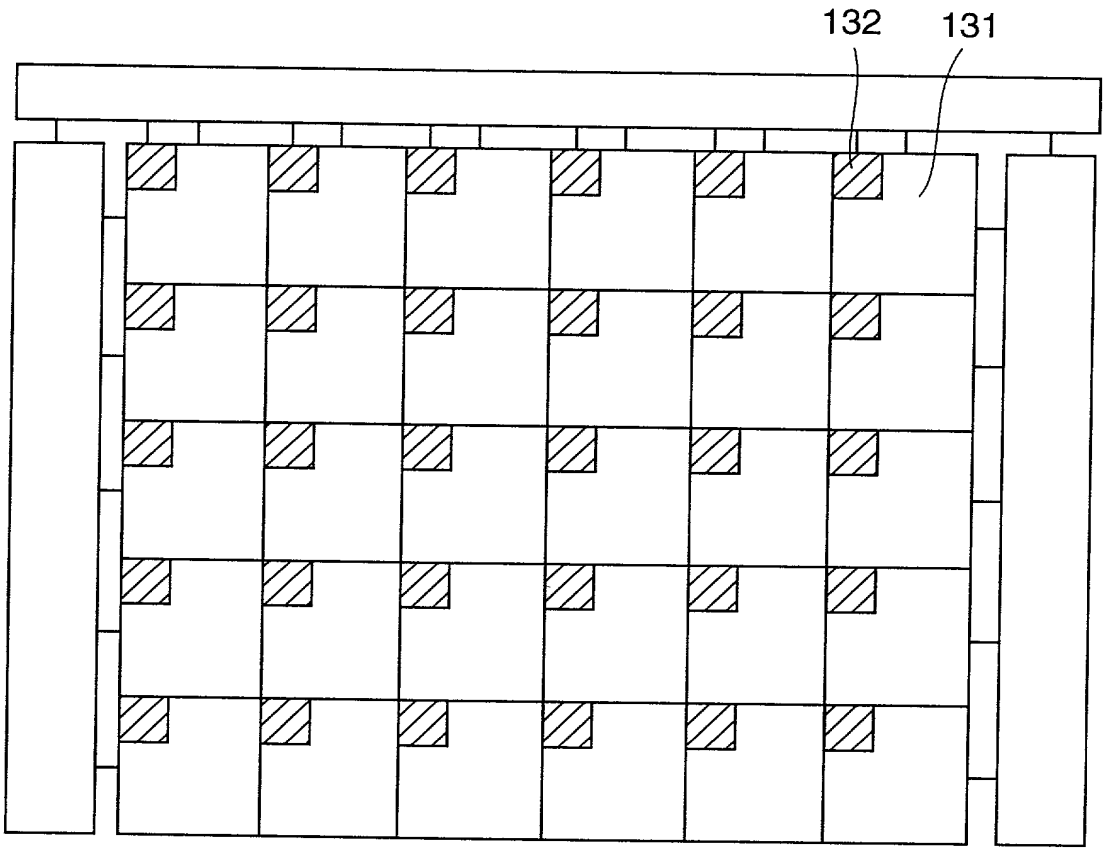


FIG.20

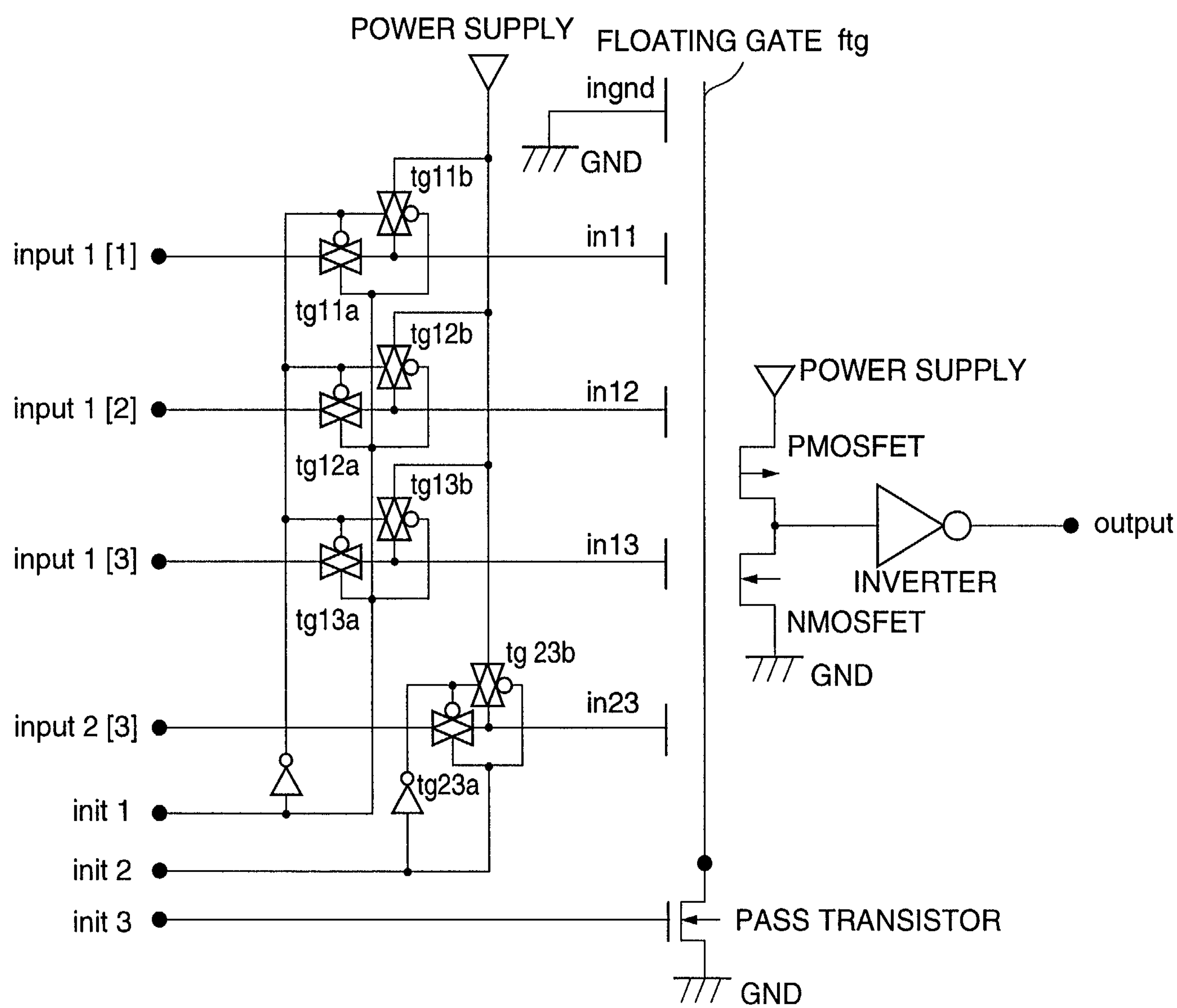

POWER SUPPLY
FLOATING GATE ftg
ingnd
GND
tg11b
in11
input 1 [1]
tg11a
tg12b
in12
input 1 [2]
tg12a
POWER SUPPLY
PMOSFET
tg13b
in13
input 1 [3]
output
tg13a
INVERTER
NMOSFET
tg 23b
GND
in23
input 2 [3]
tg23a
init 1
init 2
init 3
PASS TRANSISTOR
GND

FIG.21

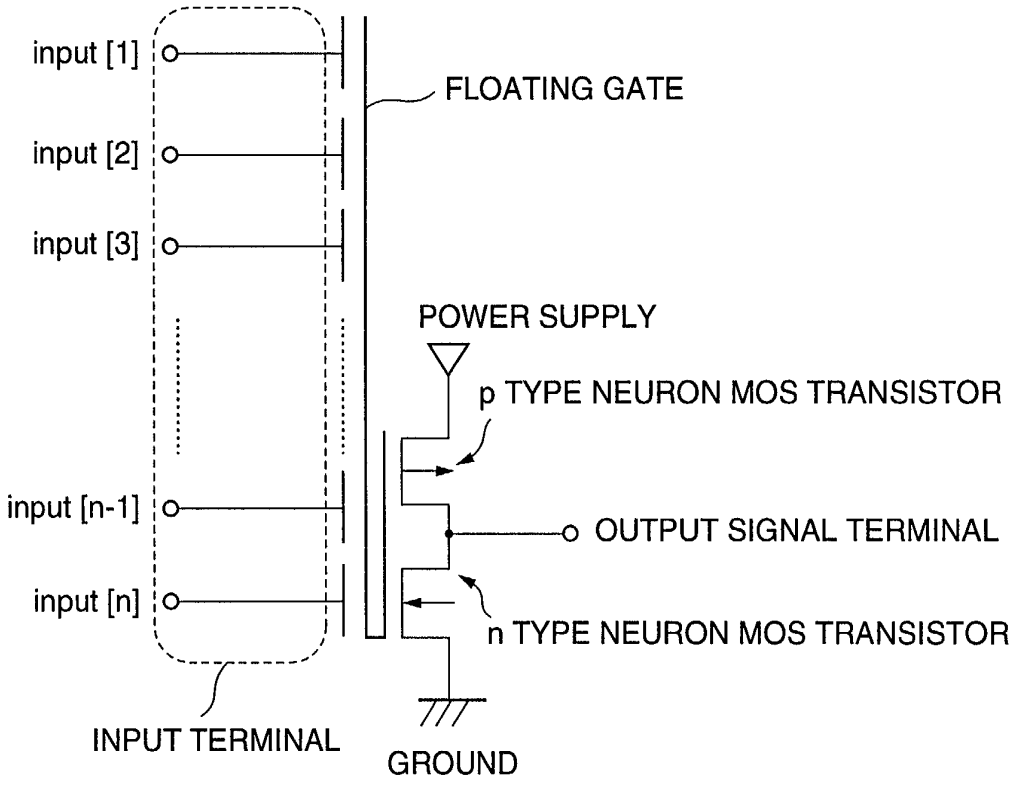

input [1]
input [2]
input [3]
input [n-1]
input [n]
FLOATING GATE
POWER SUPPLY
p TYPE NEURON MOS TRANSISTOR
OUTPUT SIGNAL TERMINAL
n TYPE NEURON MOS TRANSISTOR
INPUT TERMINAL
GROUND

FIG.22

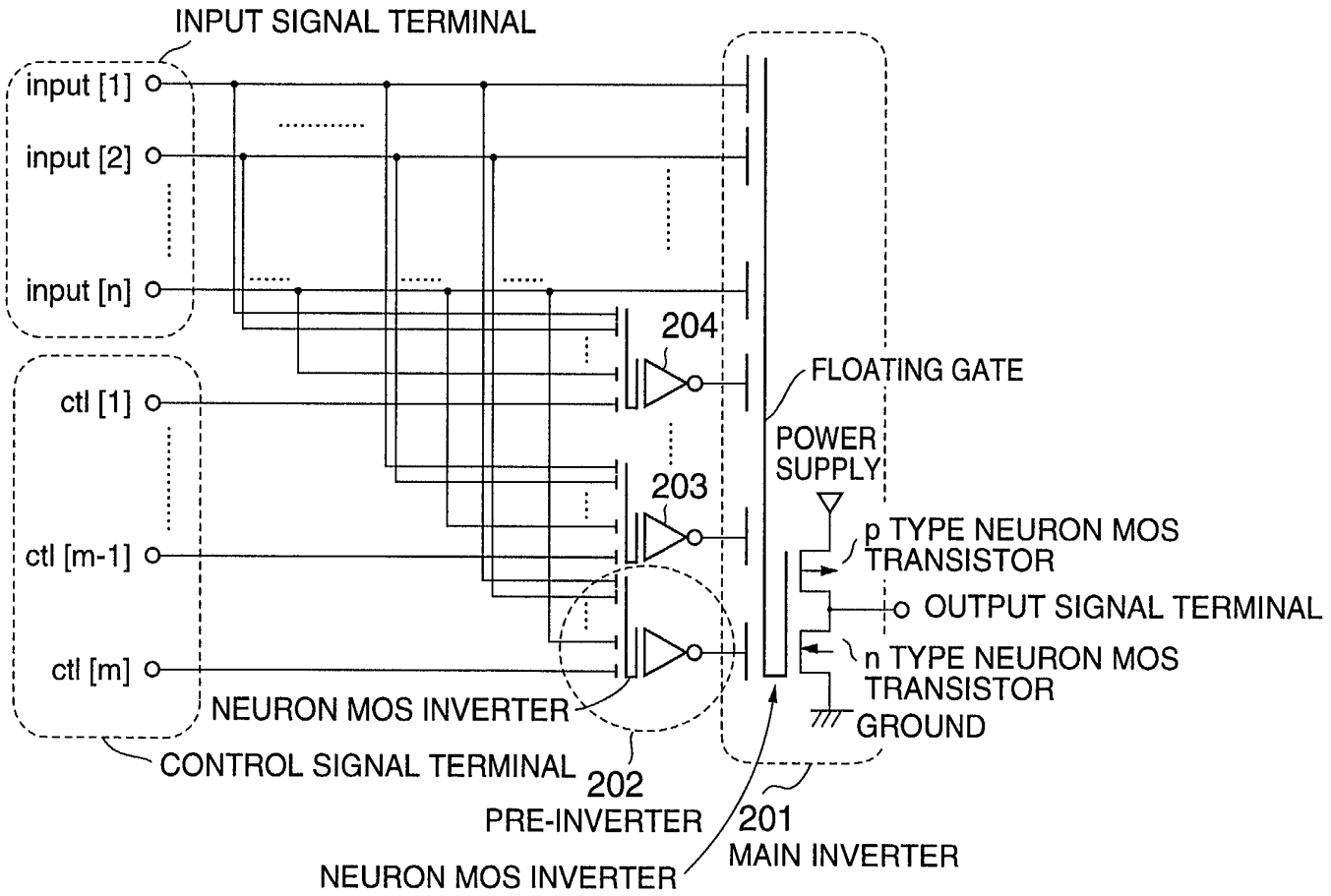

INPUT SIGNAL TERMINAL
input [1]
input [2]
input [n]
ctl [1]
ctl [m-1]
ctl [m]
204
203
FLOATING GATE
POWER SUPPLY
p TYPE NEURON MOS TRANSISTOR
OUTPUT SIGNAL TERMINAL
n TYPE NEURON MOS TRANSISTOR
GROUND
NEURON MOS INVERTER
CONTROL SIGNAL TERMINAL
202
PRE-INVERTER
201
MAIN INVERTER
NEURON MOS INVERTER

FIG.23

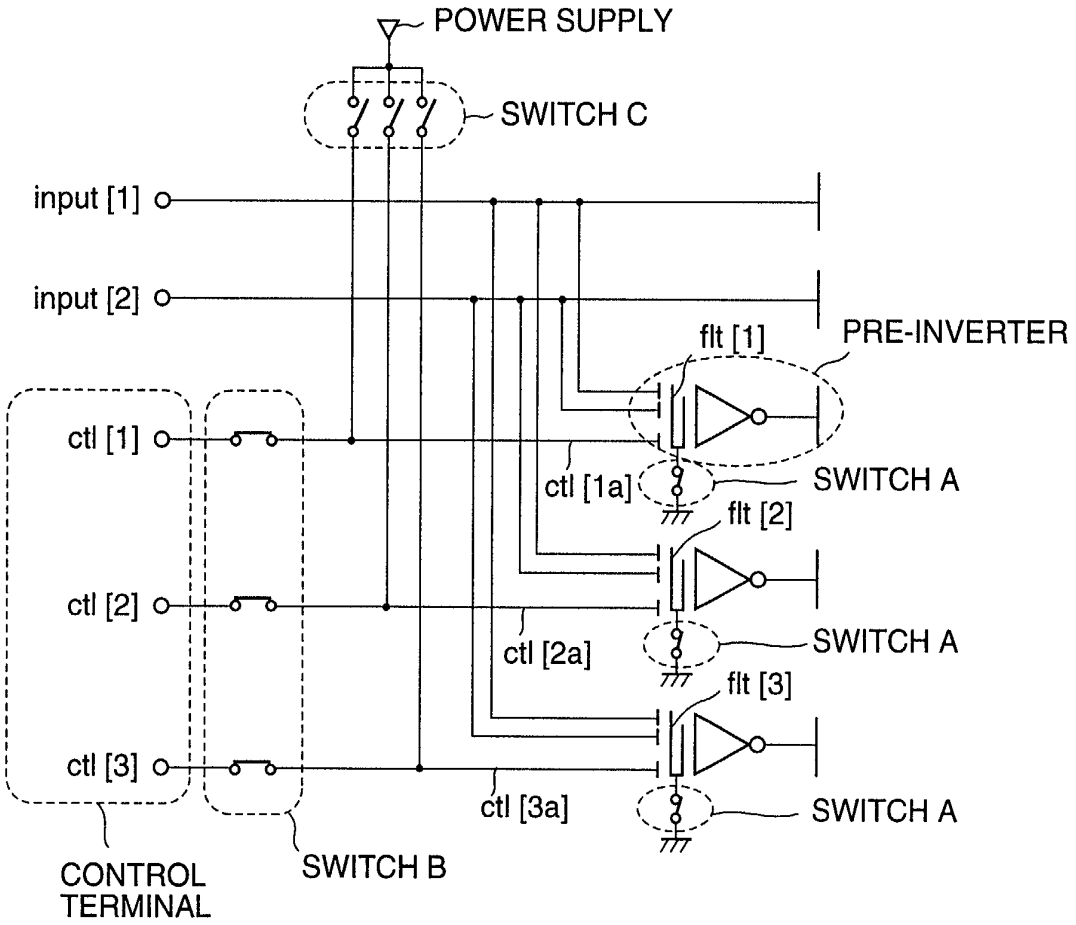

POWER SUPPLY
SWITCH C
input [1]
input [2]
flt [1]
PRE-INVERTER
ctl [1]
ctl [1a]
SWITCH A
flt [2]
ctl [2]
ctl [2a]
SWITCH A
flt [3]
ctl [3]
ctl [3a]
SWITCH A
CONTROL TERMINAL
SWITCH B

FIG.24

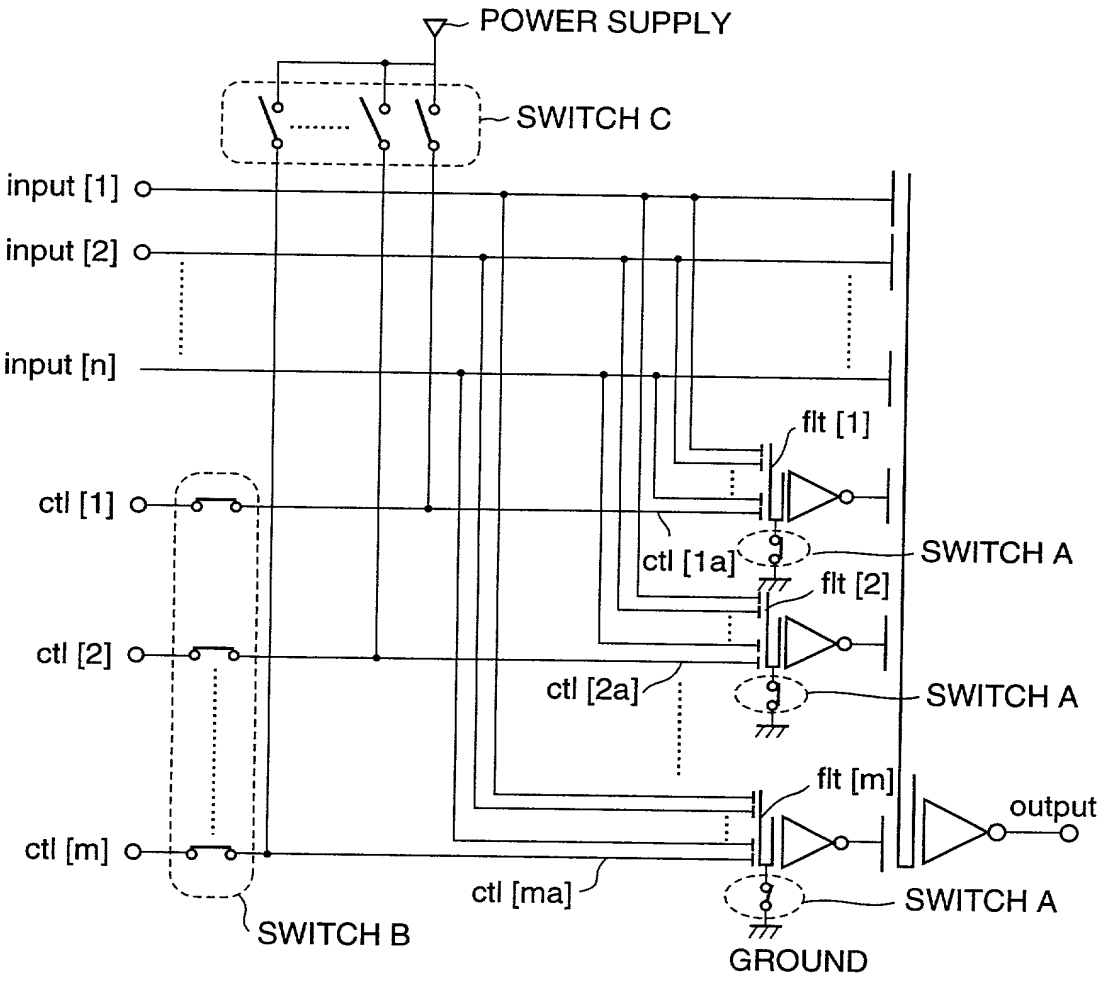

POWER SUPPLY
SWITCH C
input [1]
input [2]
input [n]
ctl [1]
ctl [2]
ctl [m]
flt [1]
ctl [1a]
SWITCH A
flt [2]
ctl [2a]
SWITCH A
flt [m]
output
ctl [ma]
SWITCH A
SWITCH B
GROUND

FIG.25

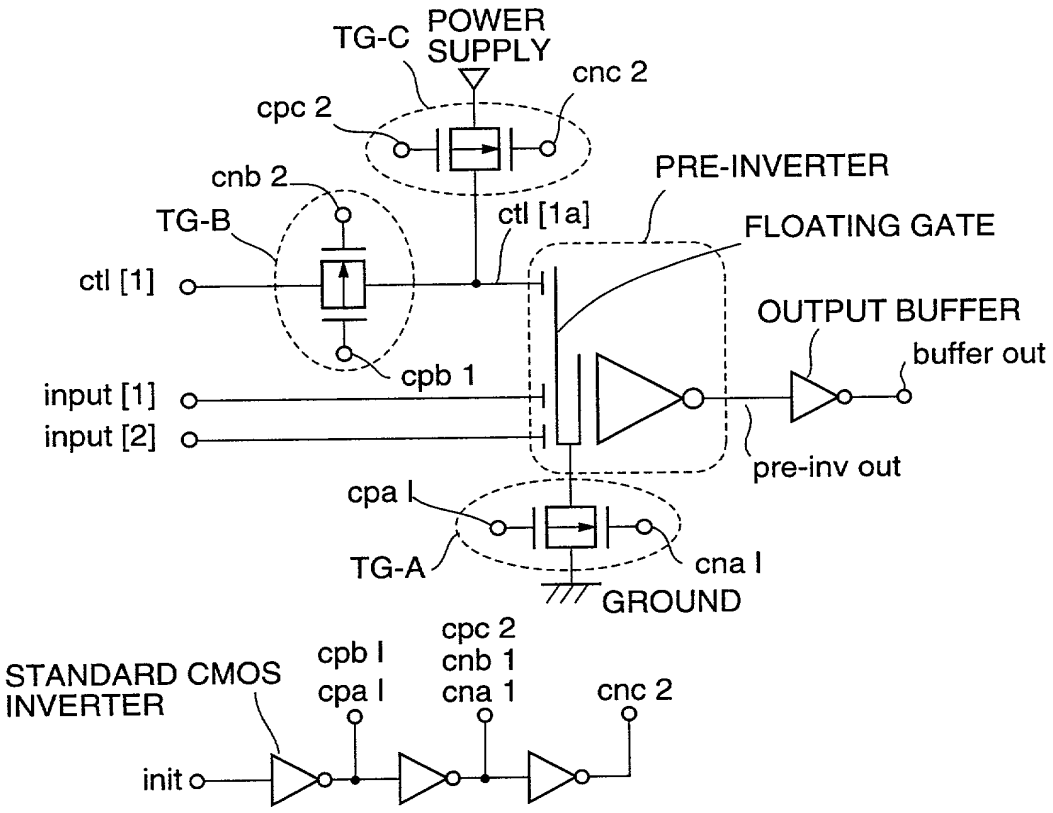

TG-C
POWER SUPPLY
cnc 2
cpc 2
PRE-INVERTER
cnb 2
TG-B
ctl [1a]
FLOATING GATE
ctl [1]
OUTPUT BUFFER
buffer out
cpb 1
input [1]
input [2]
pre-inv out
cpa l
TG-A
cna l
GROUND
STANDARD CMOS INVERTER
cpb l
cpa l
cpc 2
cnb 1
cna 1
cnc 2
init

FIG.26

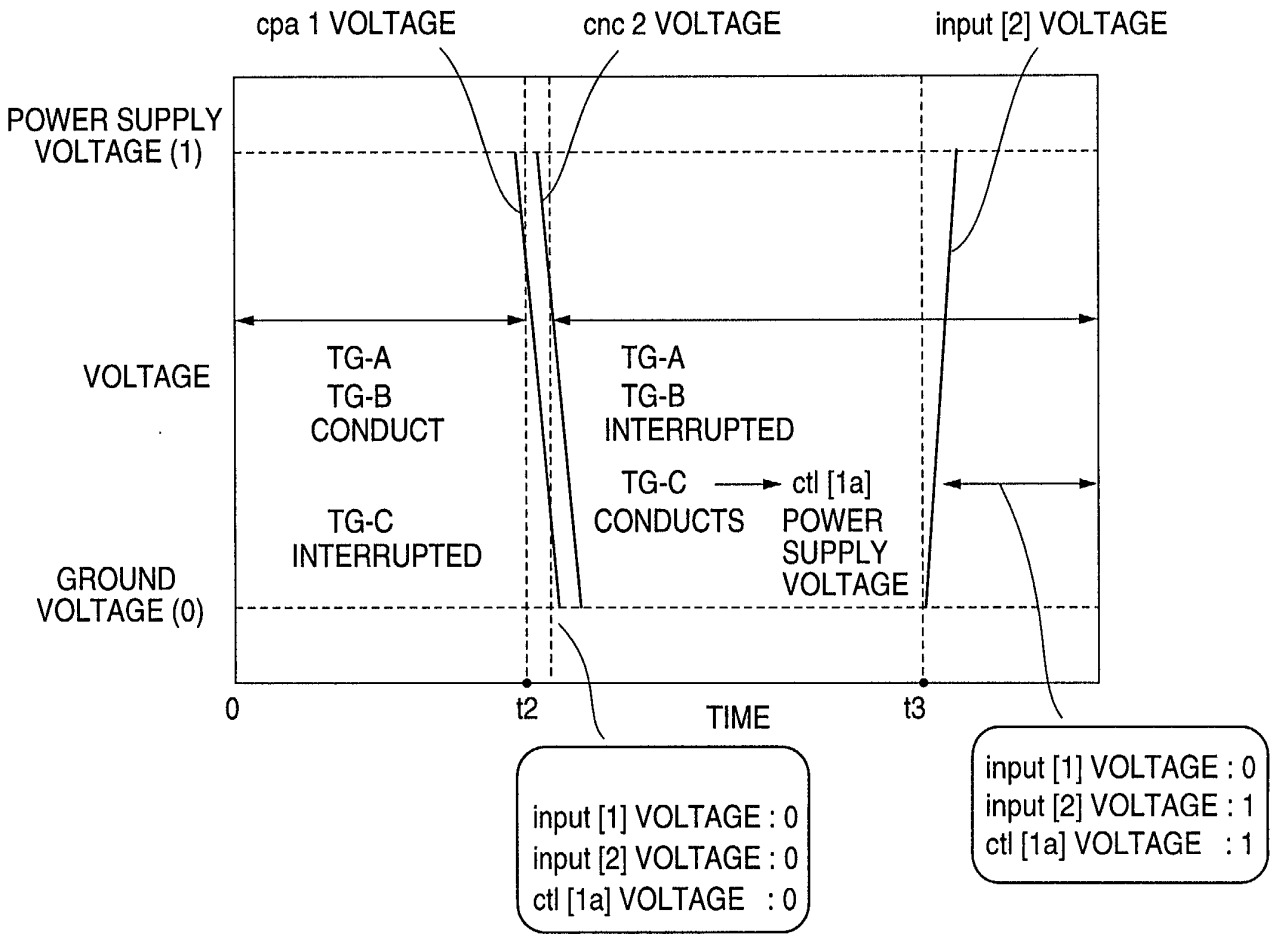


FIG.27

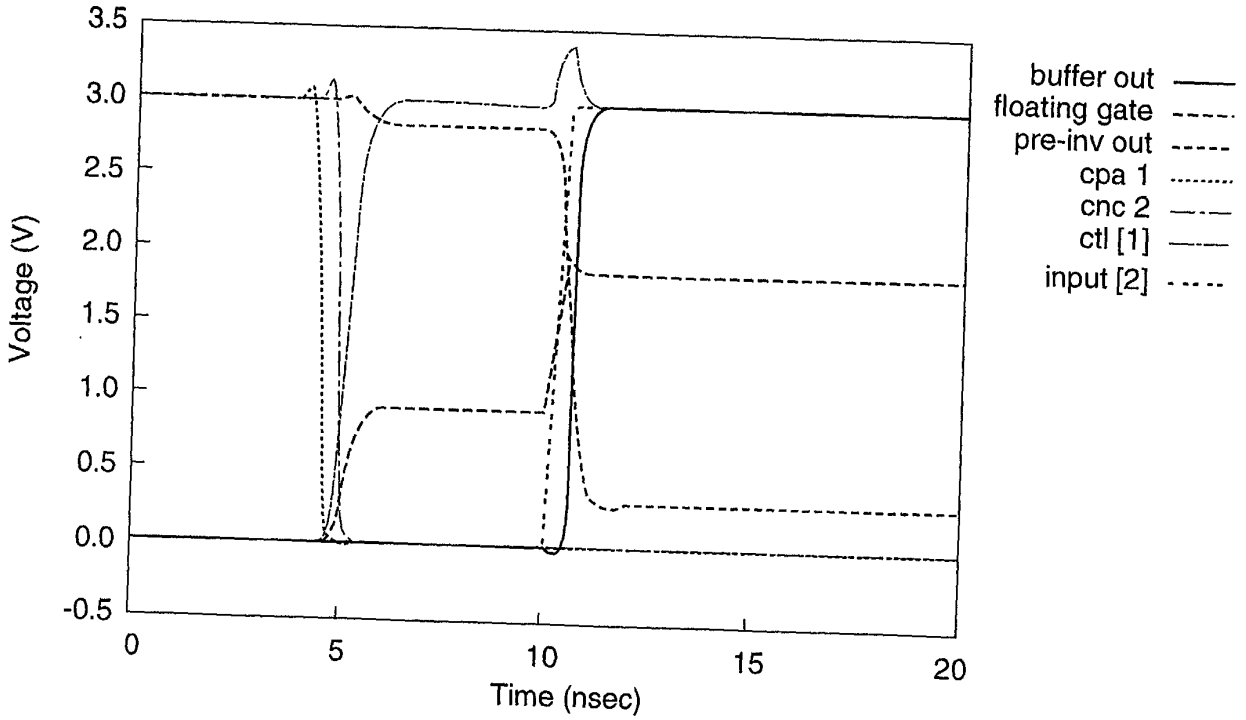


FIG.28

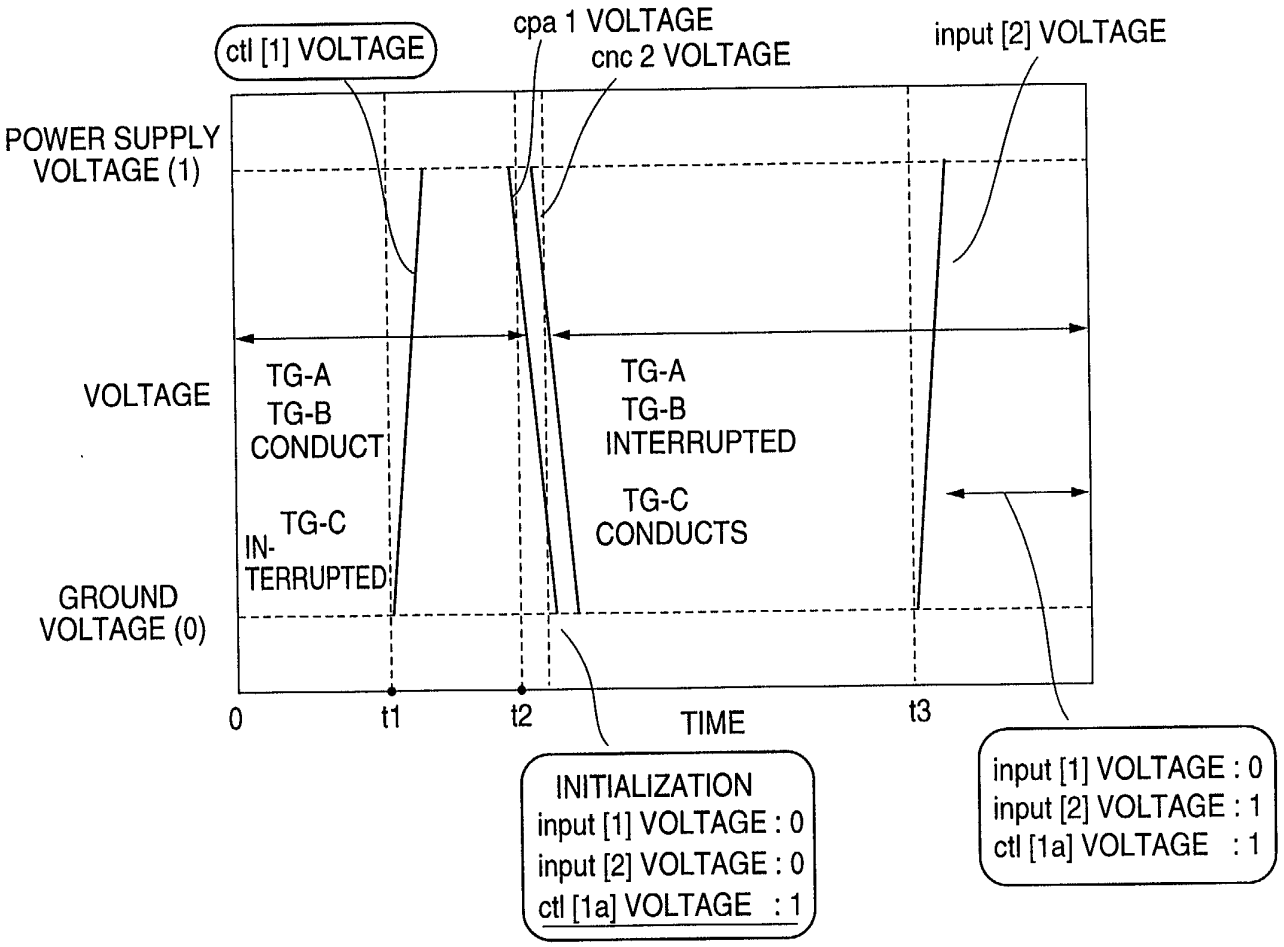

ctl [1] VOLTAGE
cpa 1 VOLTAGE
cnc 2 VOLTAGE
input [2] VOLTAGE
POWER SUPPLY VOLTAGE (1)
VOLTAGE
TG-A
TG-B
CONDUCT
TG-C
IN-
TERRUPTED
TG-A
TG-B
INTERRUPTED
TG-C
CONDUCTS
GROUND VOLTAGE (0)
0
t1
t2
TIME
t3
INITIALIZATION
input [1] VOLTAGE : 0
input [2] VOLTAGE : 0
ctl [1a] VOLTAGE : 1
input [1] VOLTAGE : 0
input [2] VOLTAGE : 1
ctl [1a] VOLTAGE : 1

FIG.29

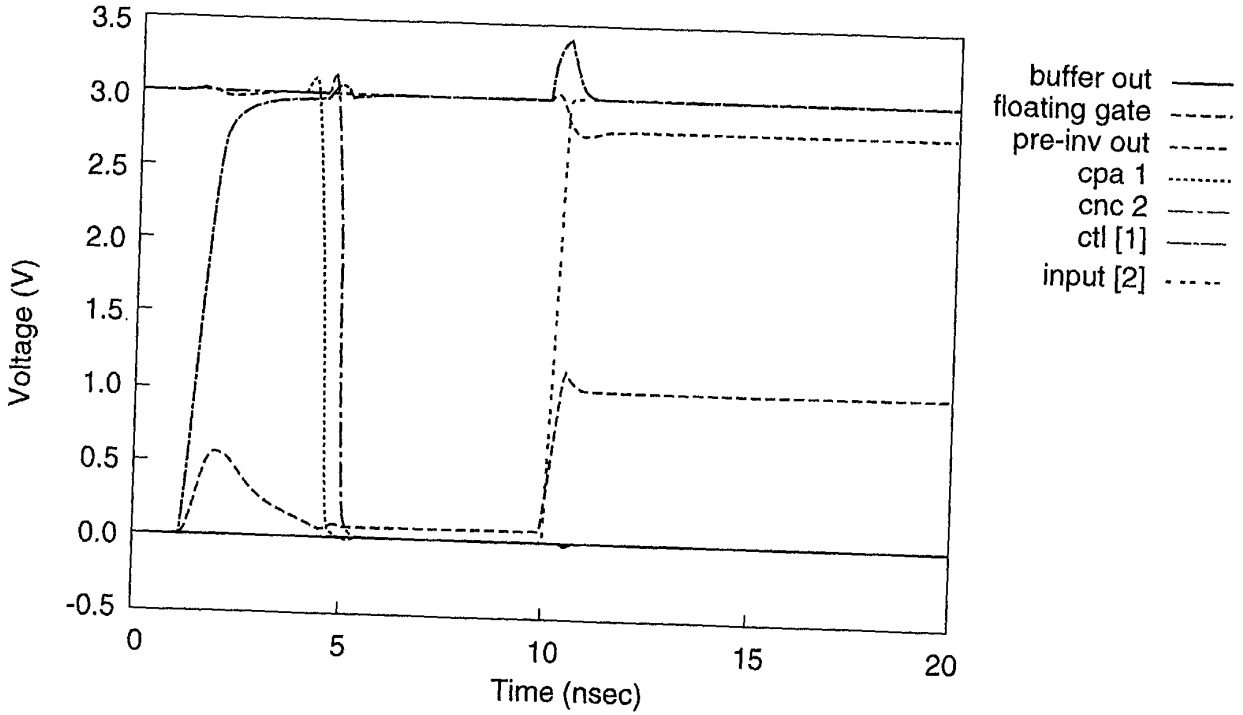


FIG.30

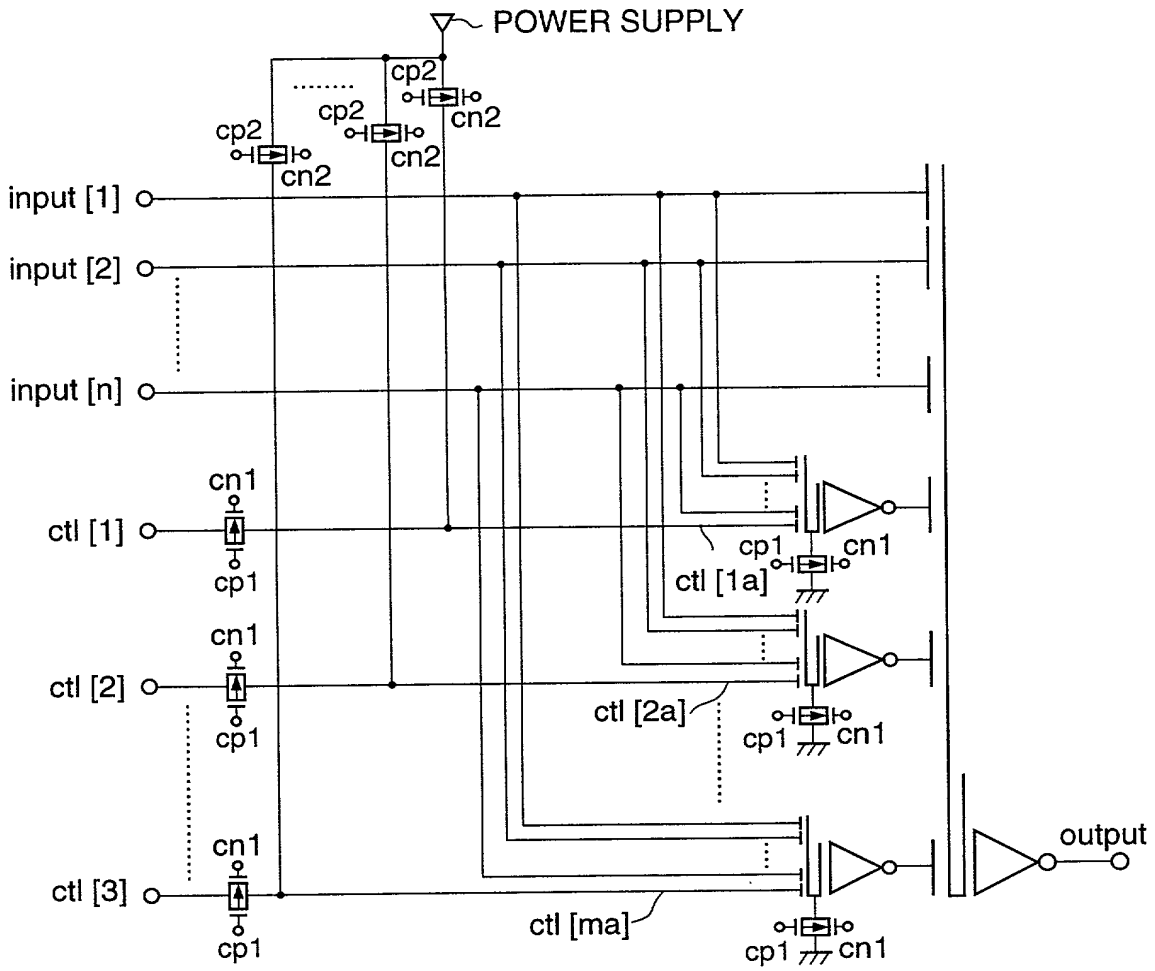

POWER SUPPLY
cp2
cn2
input [1]
input [2]
input [n]
cn1
ctl [1]
cp1
ctl [1a]
ctl [2]
ctl [2a]
ctl [3]
ctl [ma]
output

FIG.31

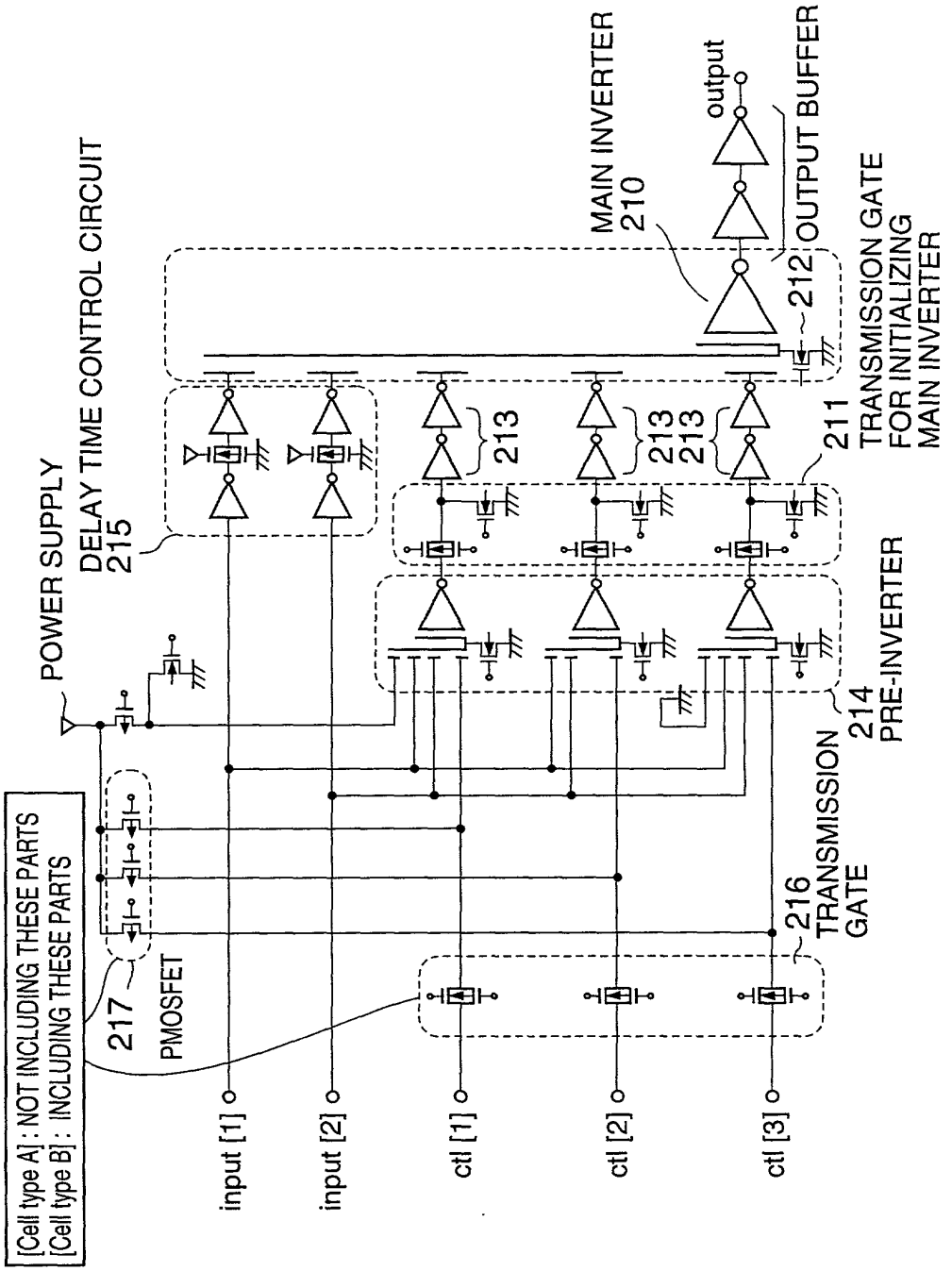

[Cell type A] : NOT INCLUDING THESE PARTS
[Cell type B] : INCLUDING THESE PARTS
POWER SUPPLY
DELAY TIME CONTROL CIRCUIT
215
217
PMOSFET
input [1]
input [2]
ctl [1]
ctl [2]
ctl [3]
216
TRANSMISSION GATE
214
PRE-INVERTER
213
213
213
211
TRANSMISSION GATE FOR INITIALIZING MAIN INVERTER
MAIN INVERTER
210
212
OUTPUT BUFFER
output

FIG.32

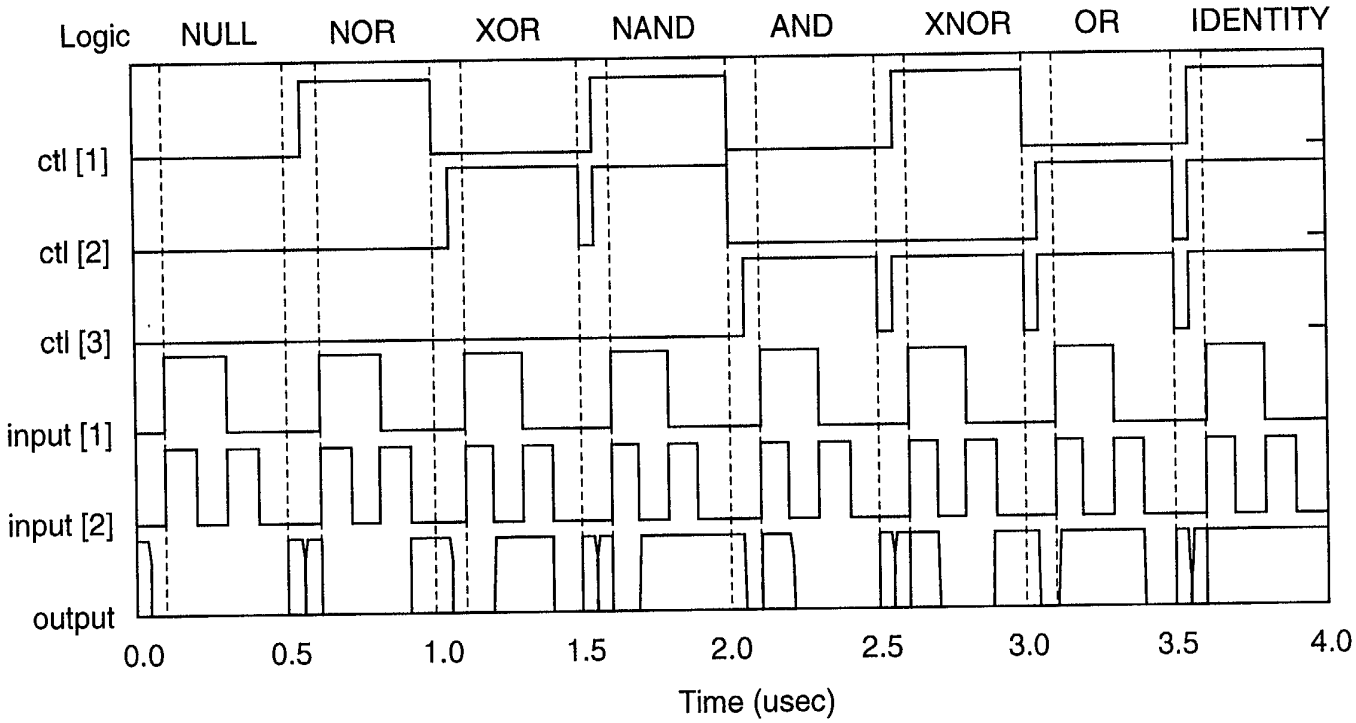


FIG.33

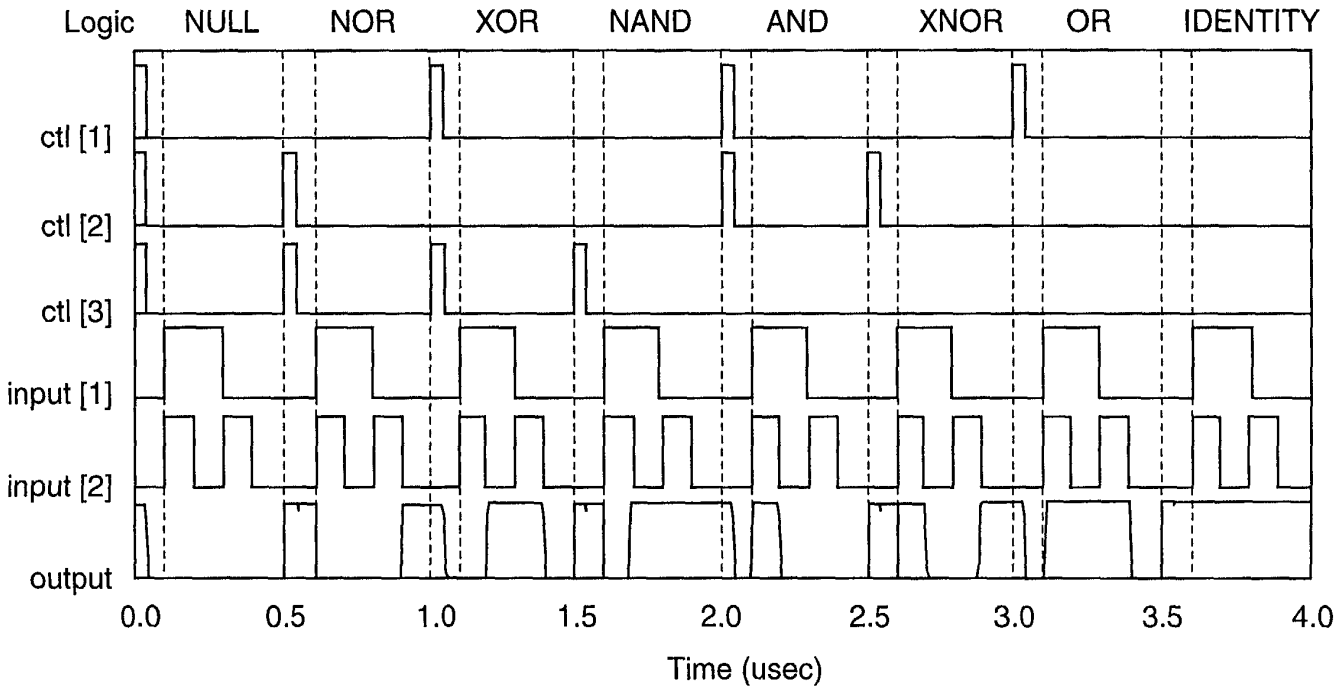


FIG.34

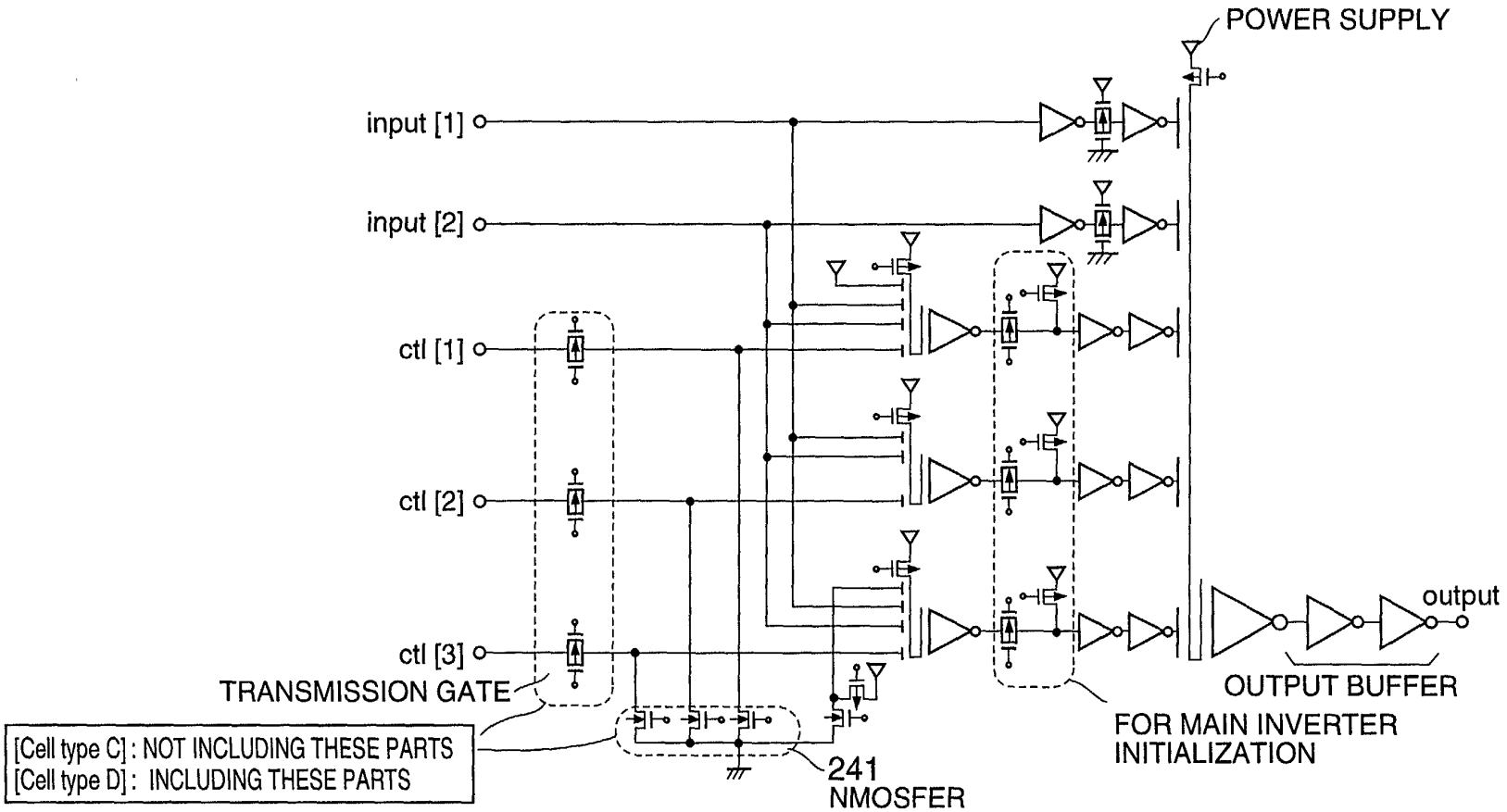


FIG.35

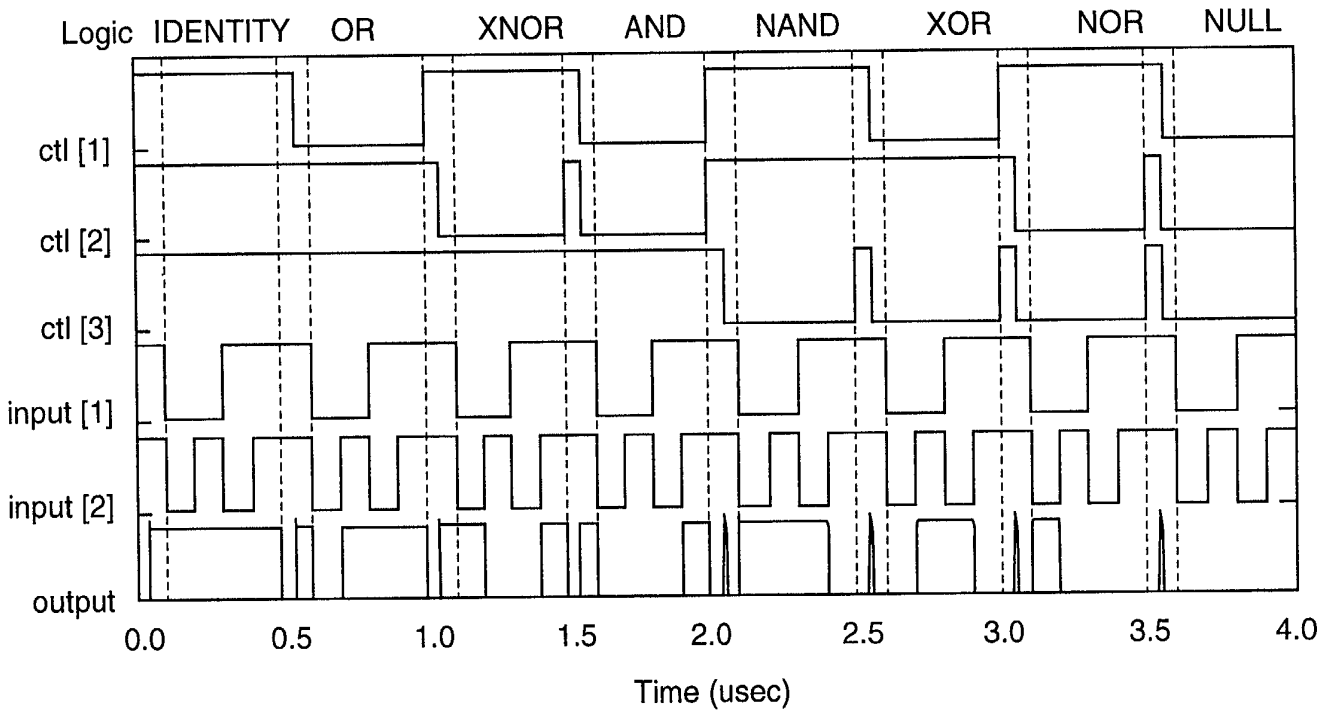


FIG.36

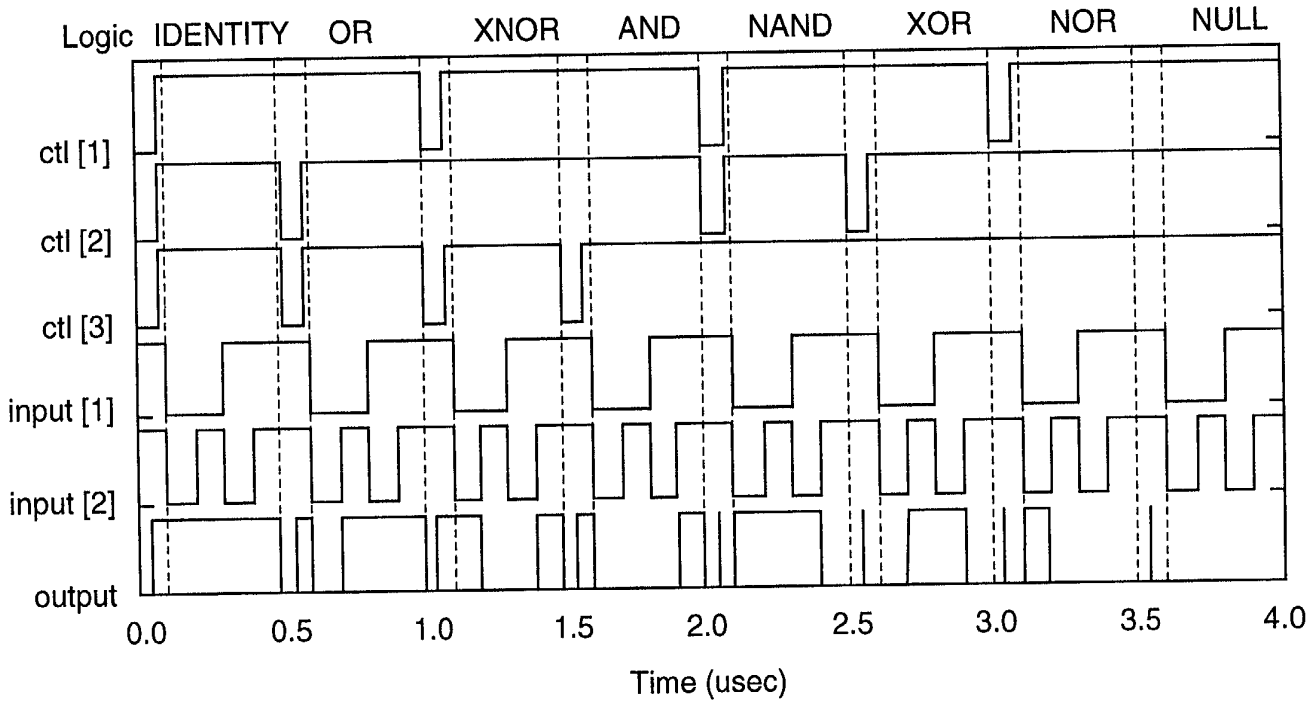

Logic
IDENTITY
OR
XNOR
AND
NAND
XOR
NOR
NULL
ctl [1]
ctl [2]
ctl [3]
input [1]
input [2]
output
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Time (usec)

FIG.37

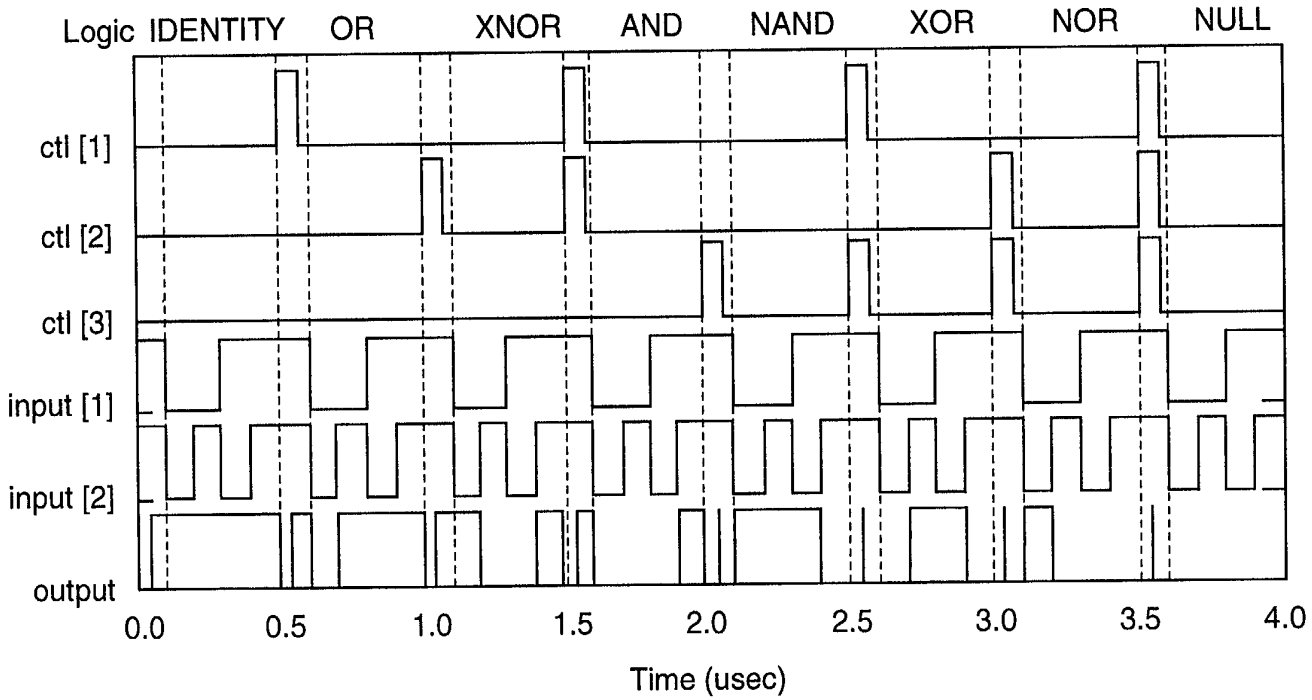


FIG.38

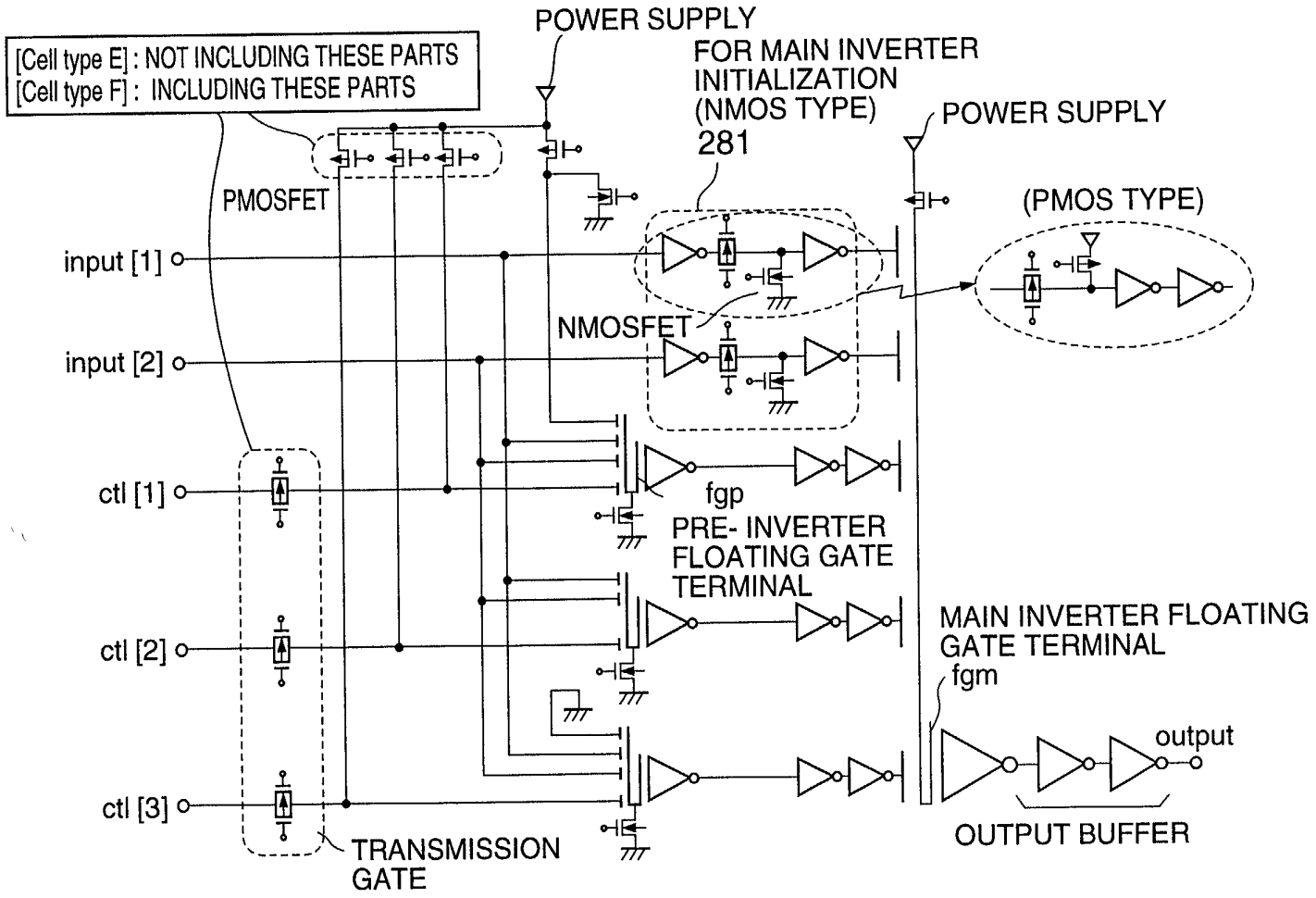


FIG.39

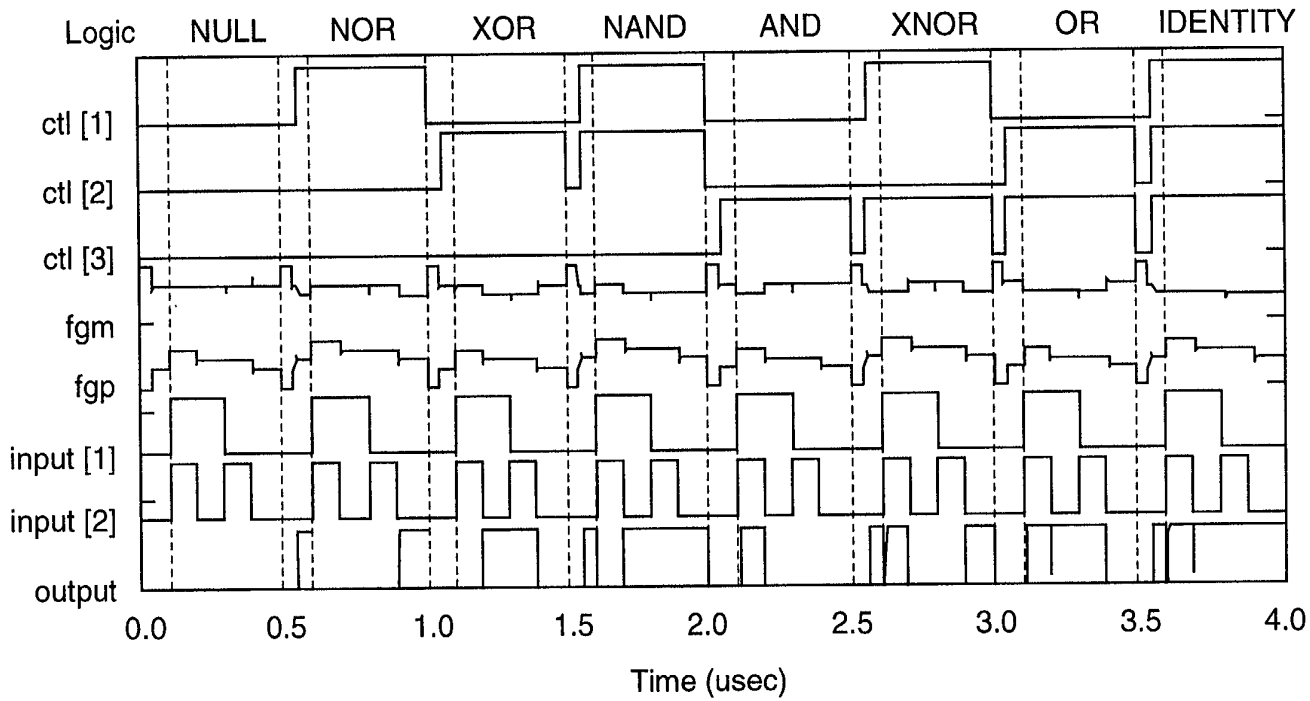


FIG.40

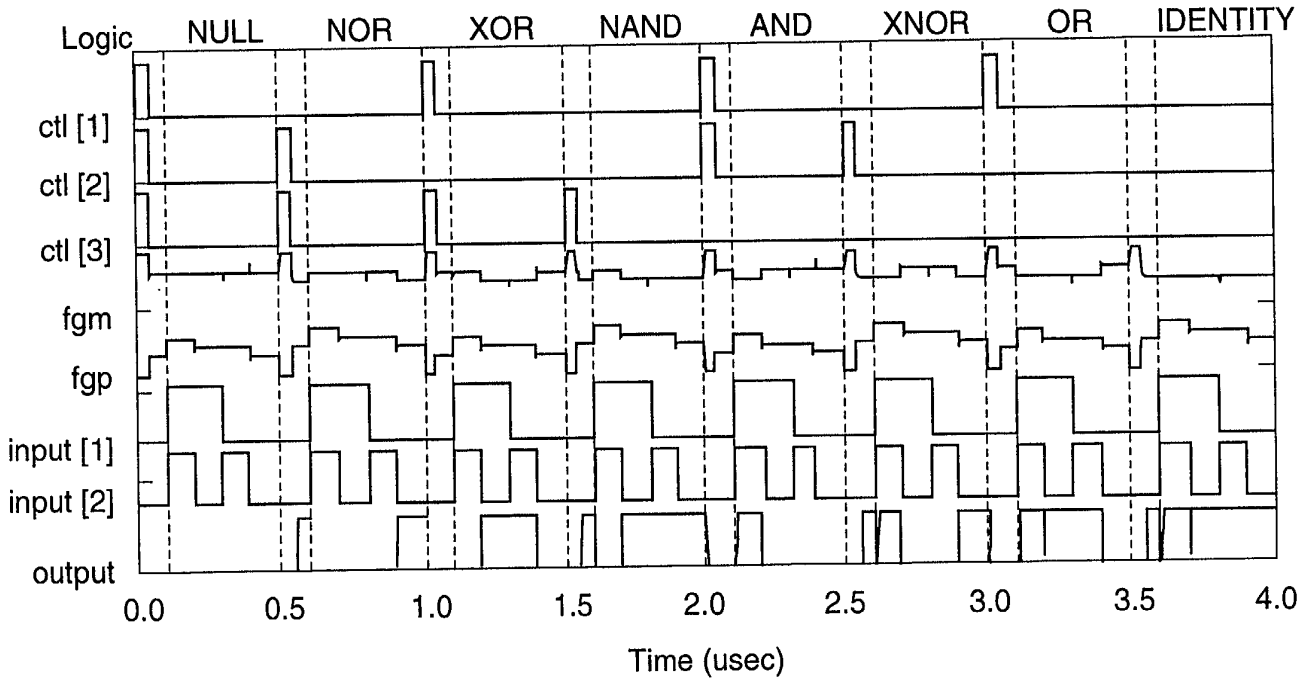

Logic
NULL
NOR
XOR
NAND
AND
XNOR
OR
IDENTITY
ctl [1]
ctl [2]
ctl [3]
fgm
fgp
input [1]
input [2]
output
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Time (usec)

FIG.41

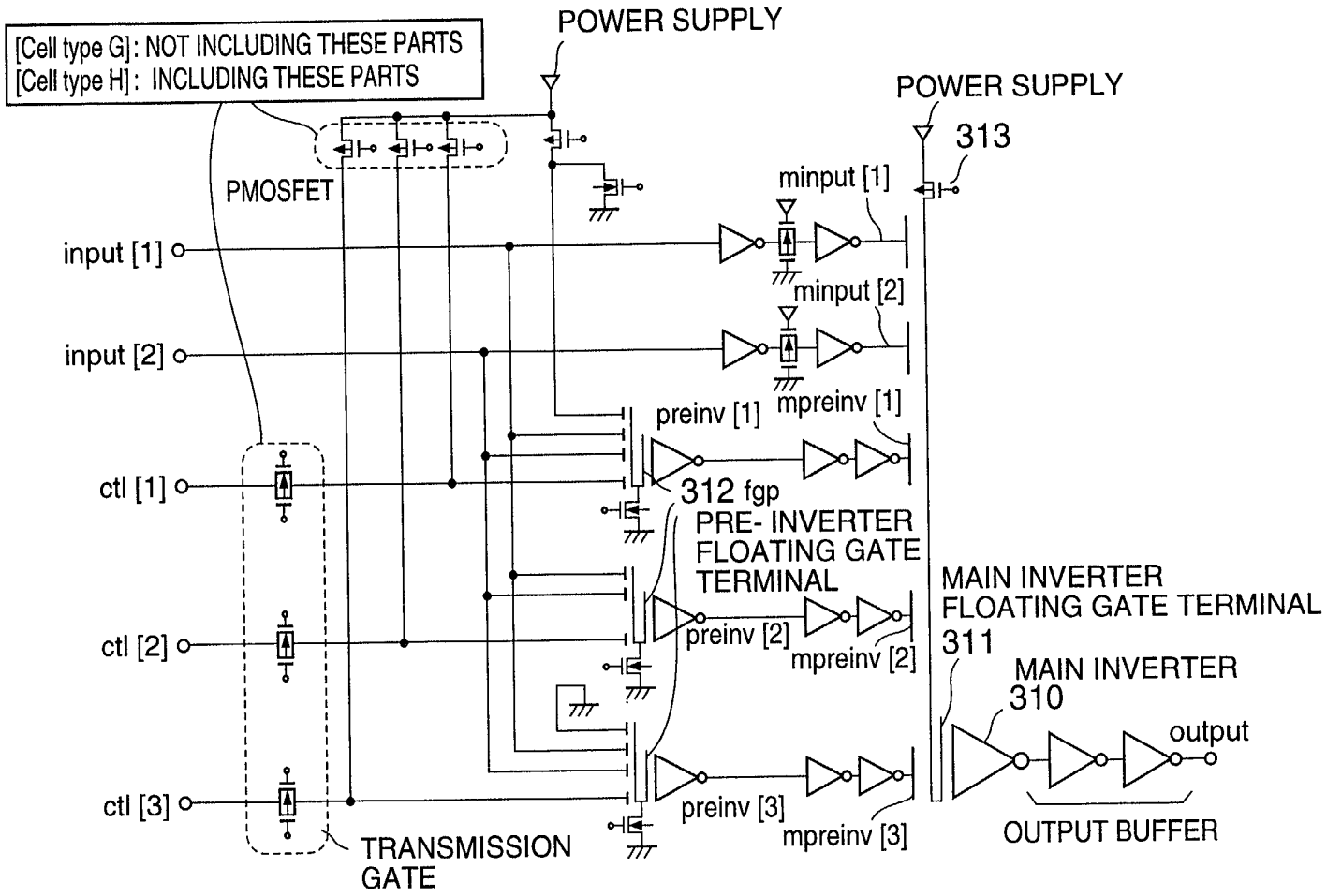
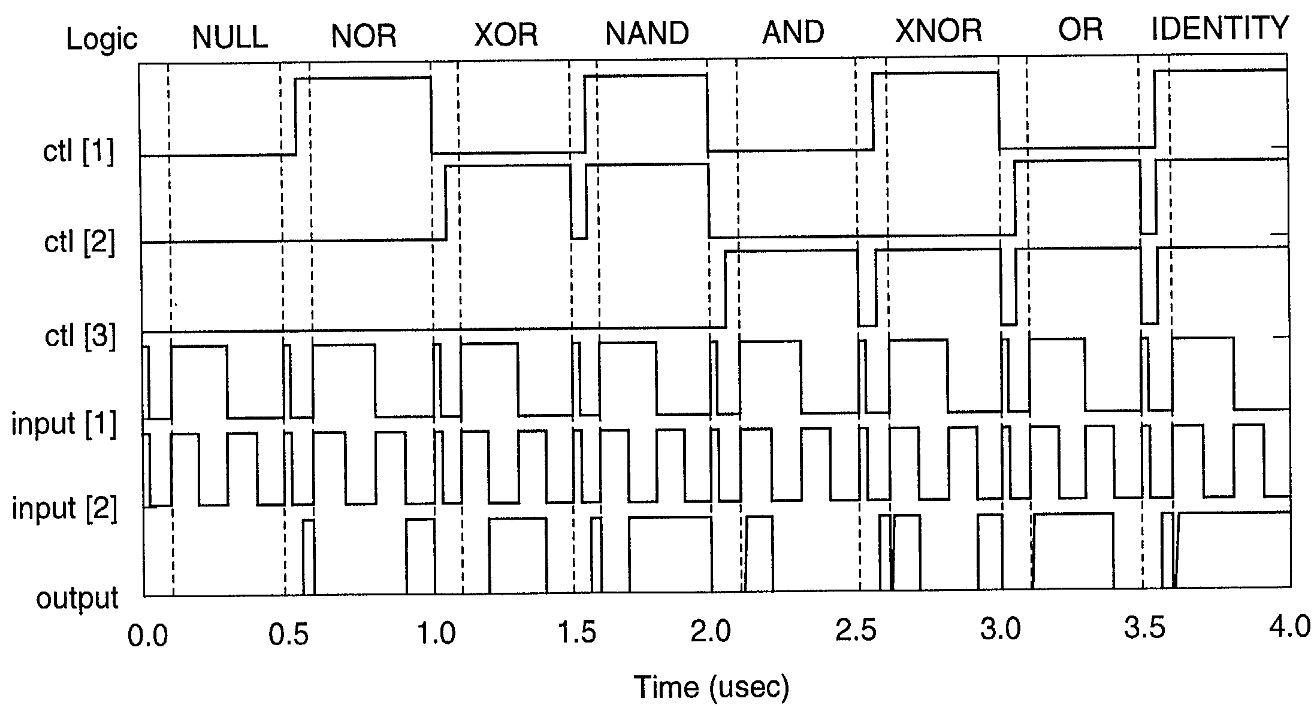


FIG.42



Logic
NULL
NOR
XOR
NAND
AND
XNOR
OR
IDENTITY
ctl [1]
ctl [2]
ctl [3]
input [1]
input [2]
output
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Time (usec)

FIG.43

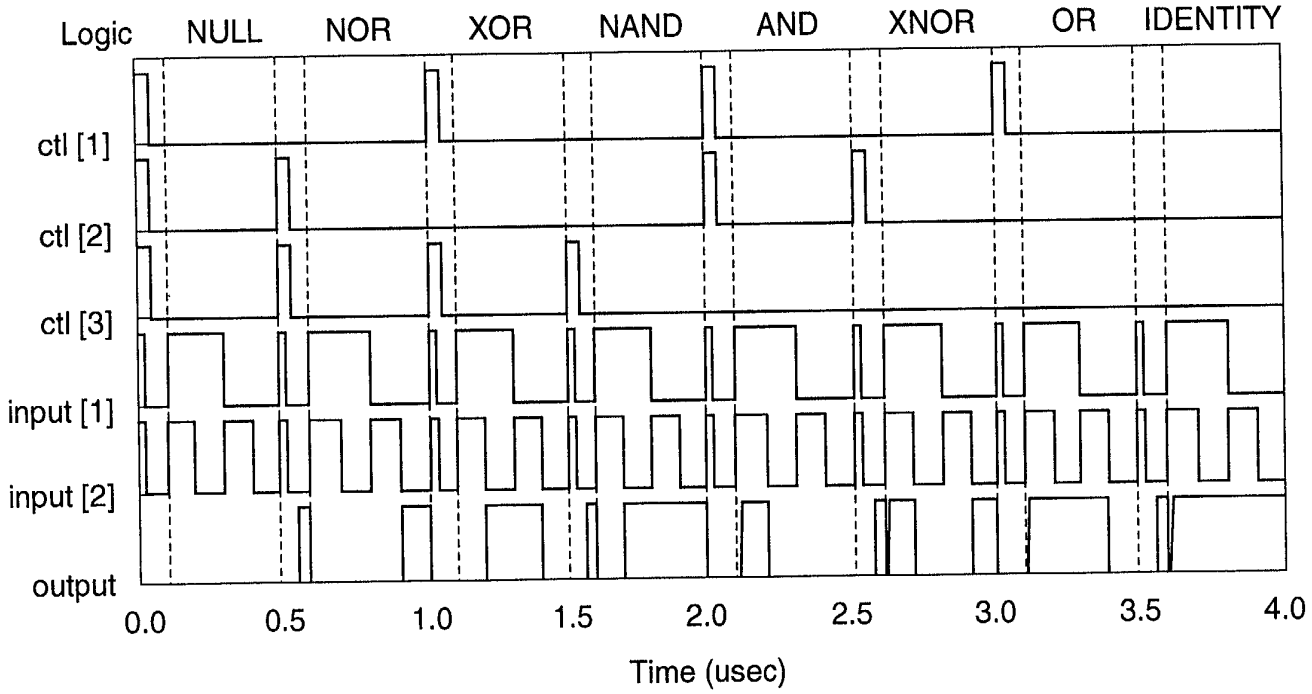


FIG.44

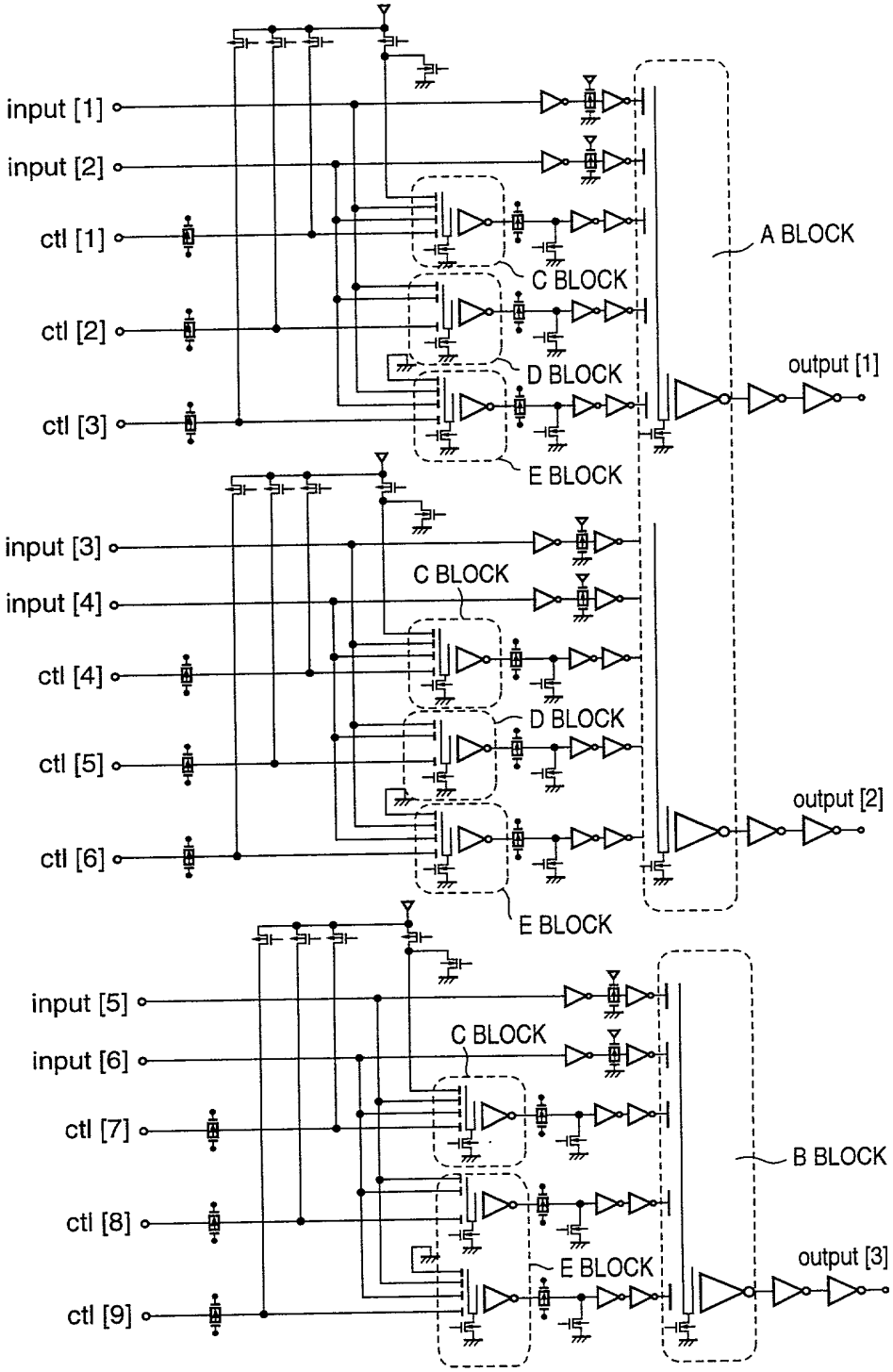

input [1]
input [2]
ctl [1]
ctl [2]
ctl [3]
A BLOCK
C BLOCK
D BLOCK
E BLOCK
output [1]
input [3]
input [4]
ctl [4]
ctl [5]
ctl [6]
C BLOCK
D BLOCK
E BLOCK
output [2]
input [5]
input [6]
ctl [7]
ctl [8]
ctl [9]
C BLOCK
B BLOCK
E BLOCK
output [3]

FIG.45

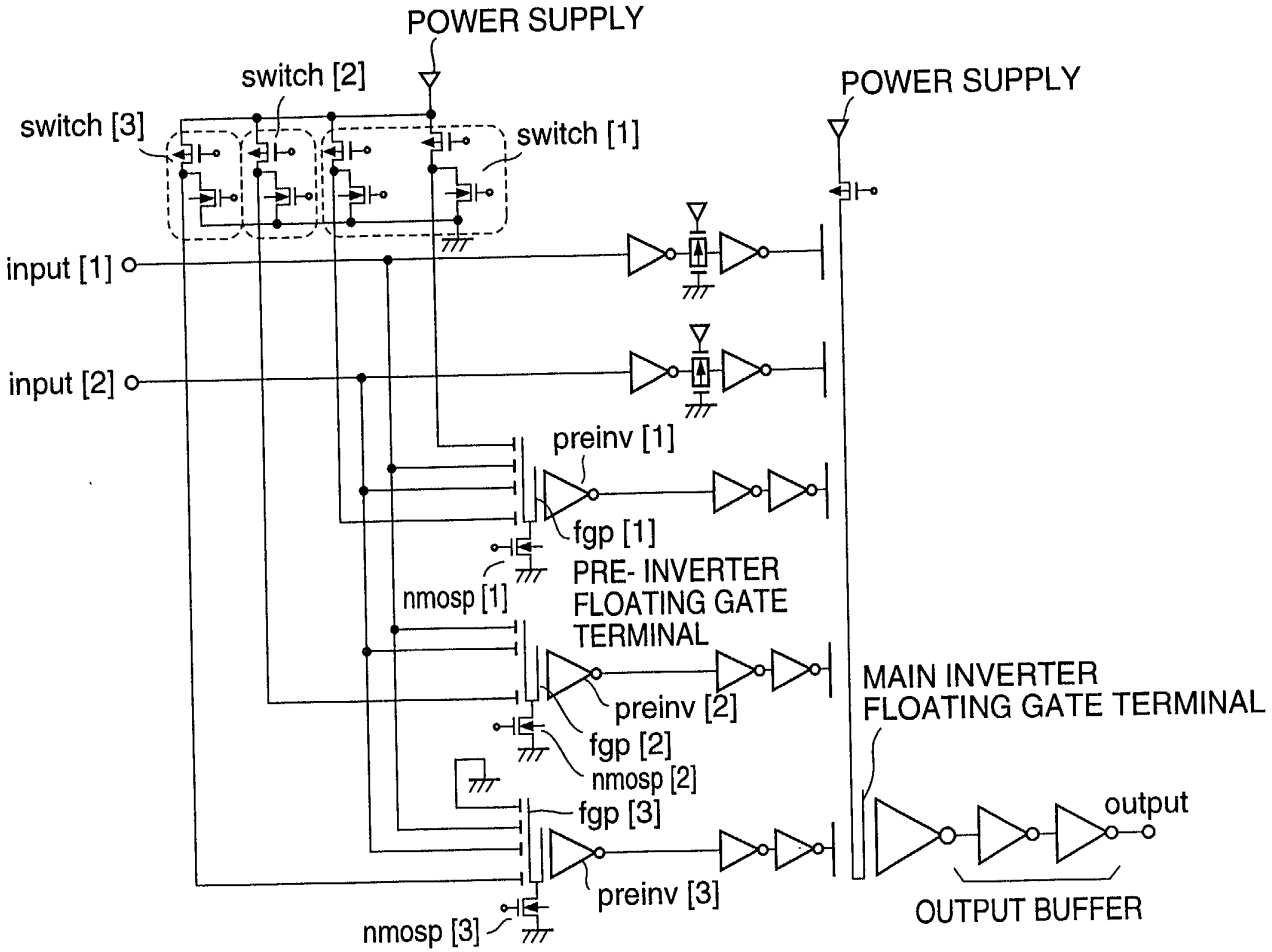


FIG.46

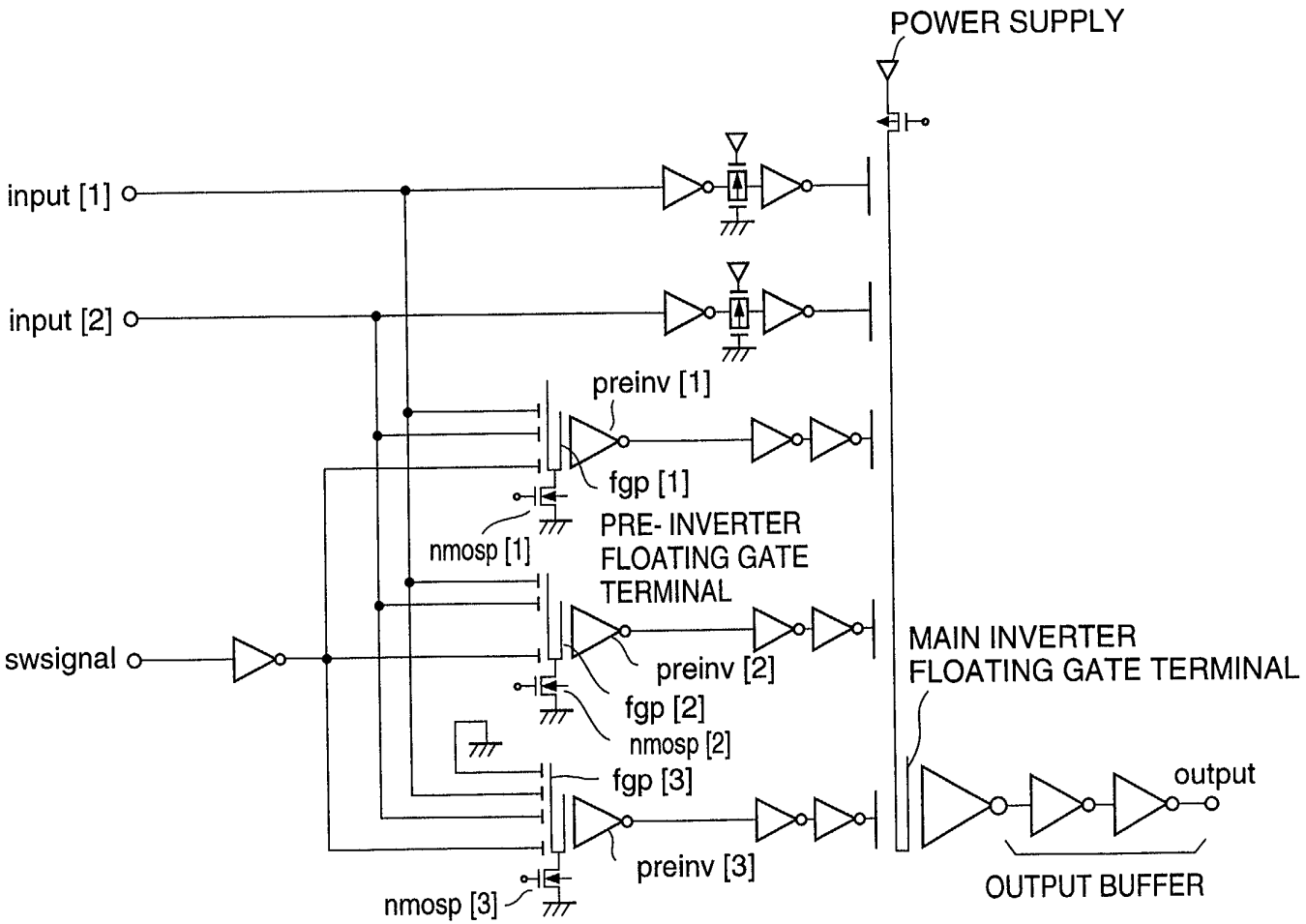


FIG.47

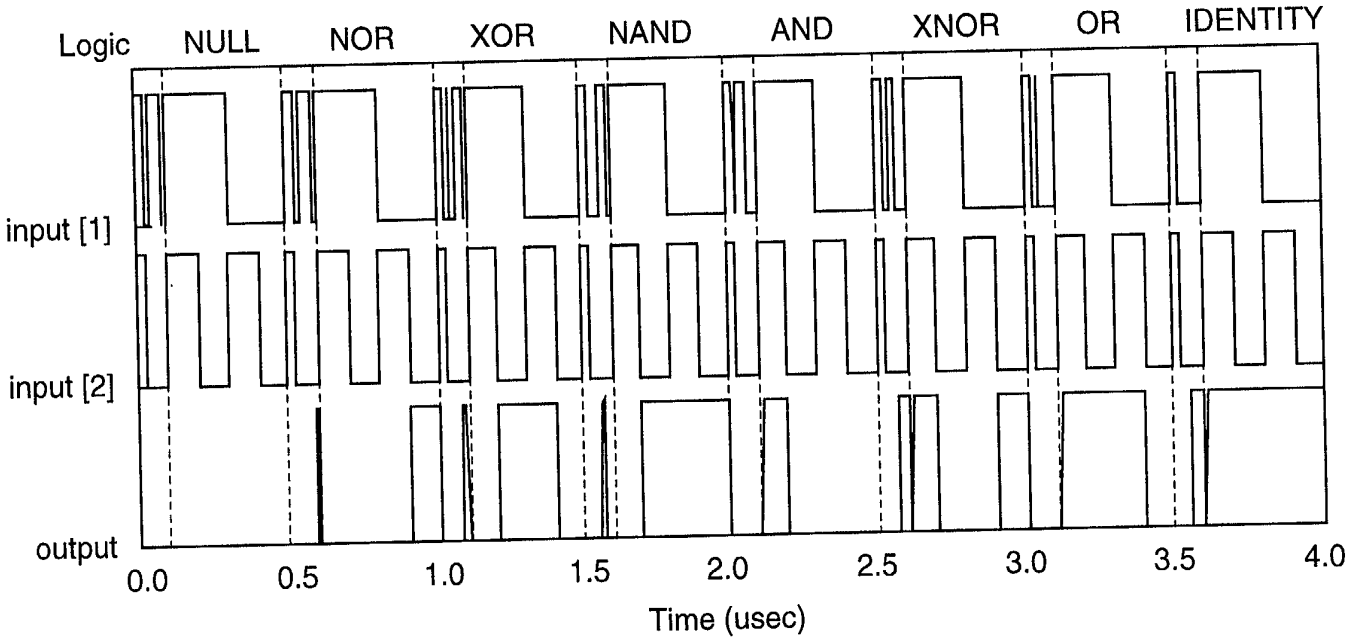


FIG.48A

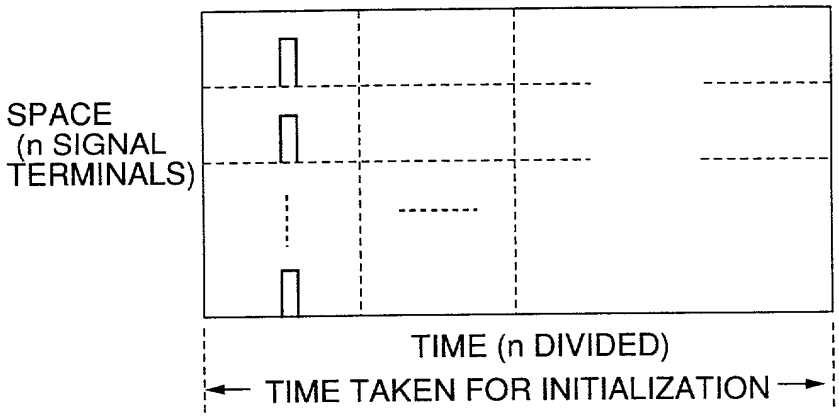


FIG.48B

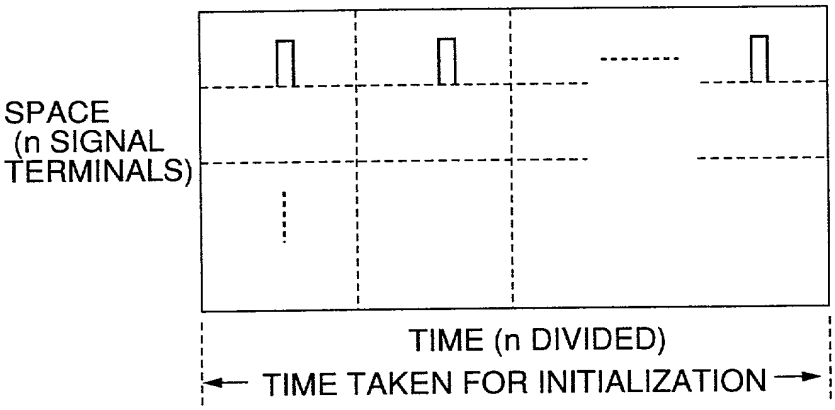


FIG.48C

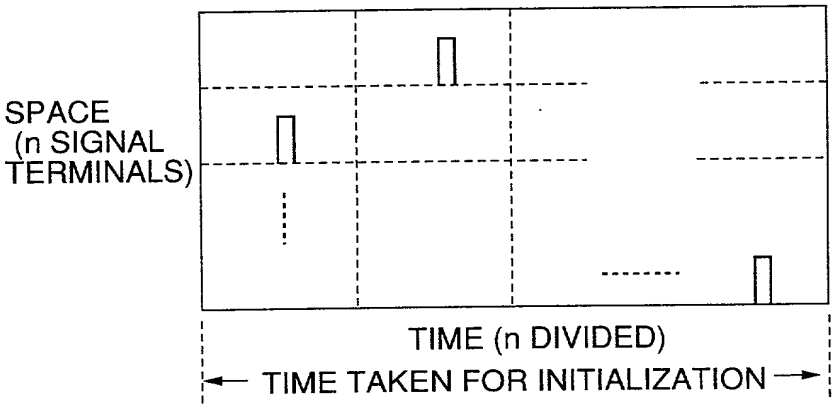


FIG.49A

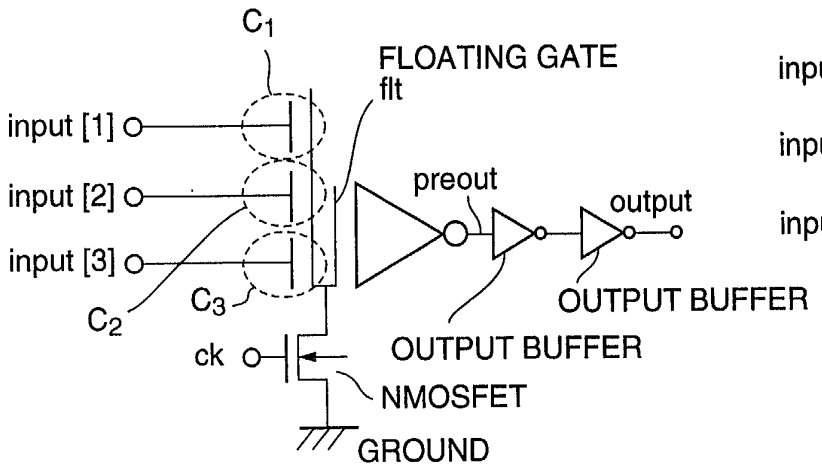


FIG.49B

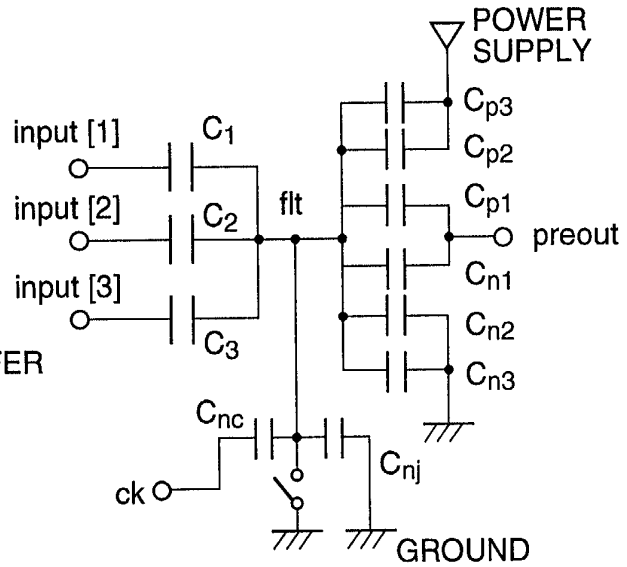


FIG.50

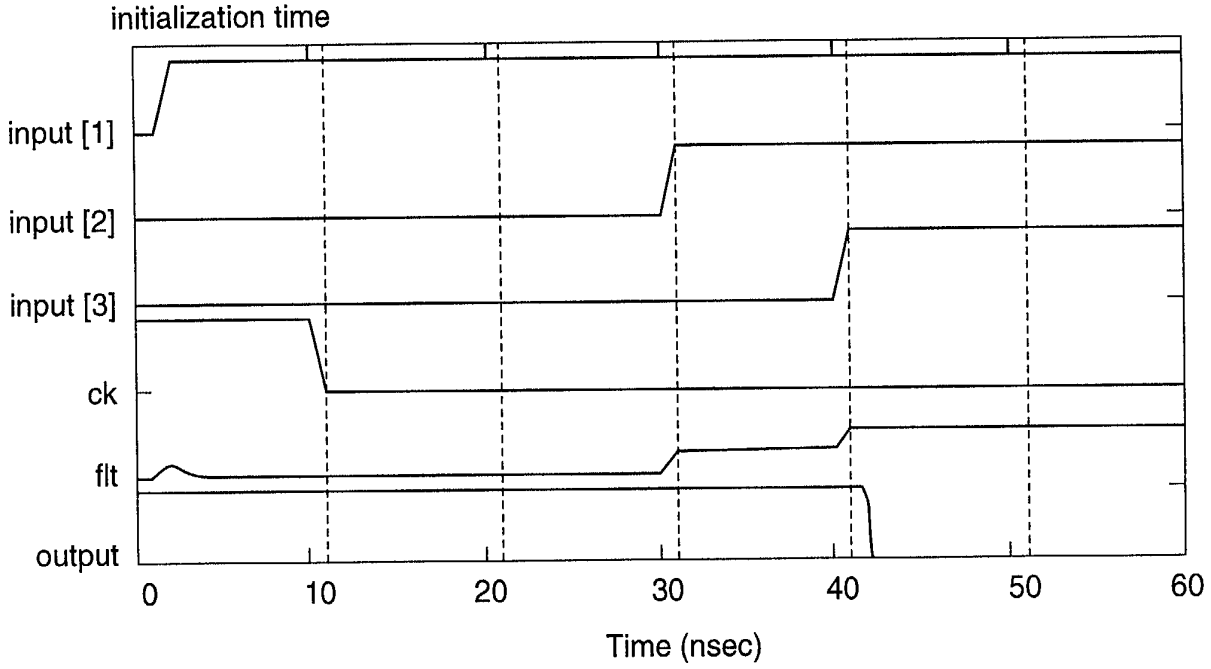

initialization time
input [1]
input [2]
input [3]
ck
flt
output
0
10
20
30
40
50
60
Time (nsec)

FIG.51

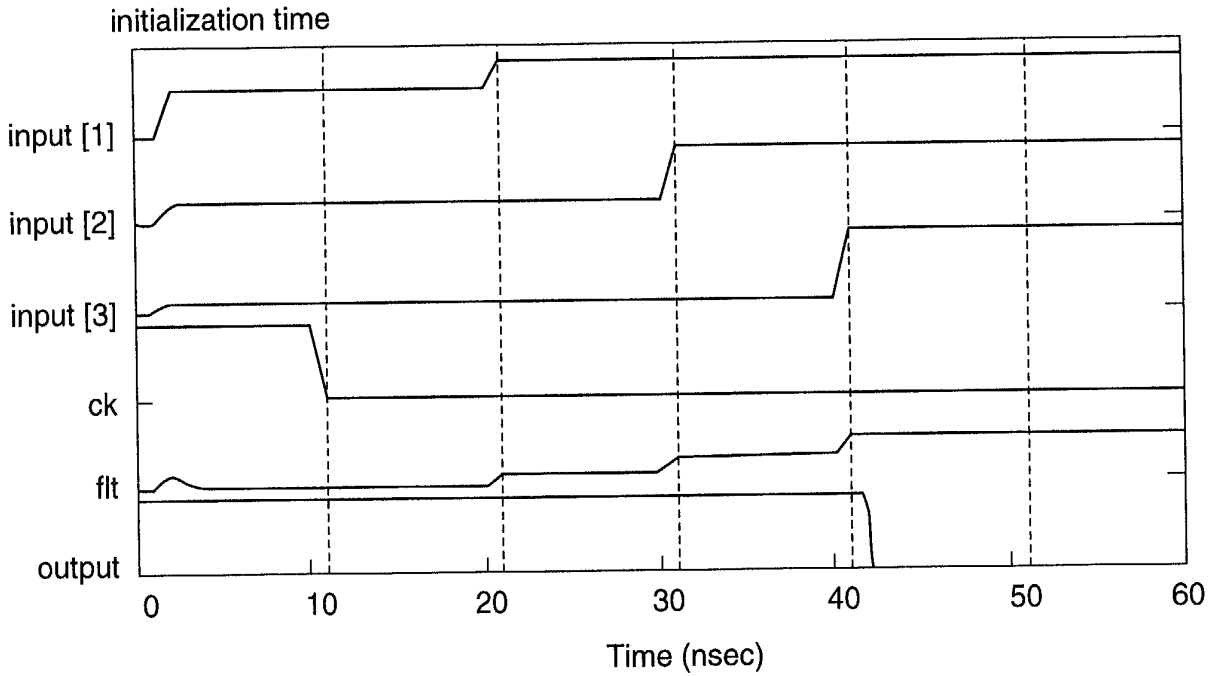


FIG.52

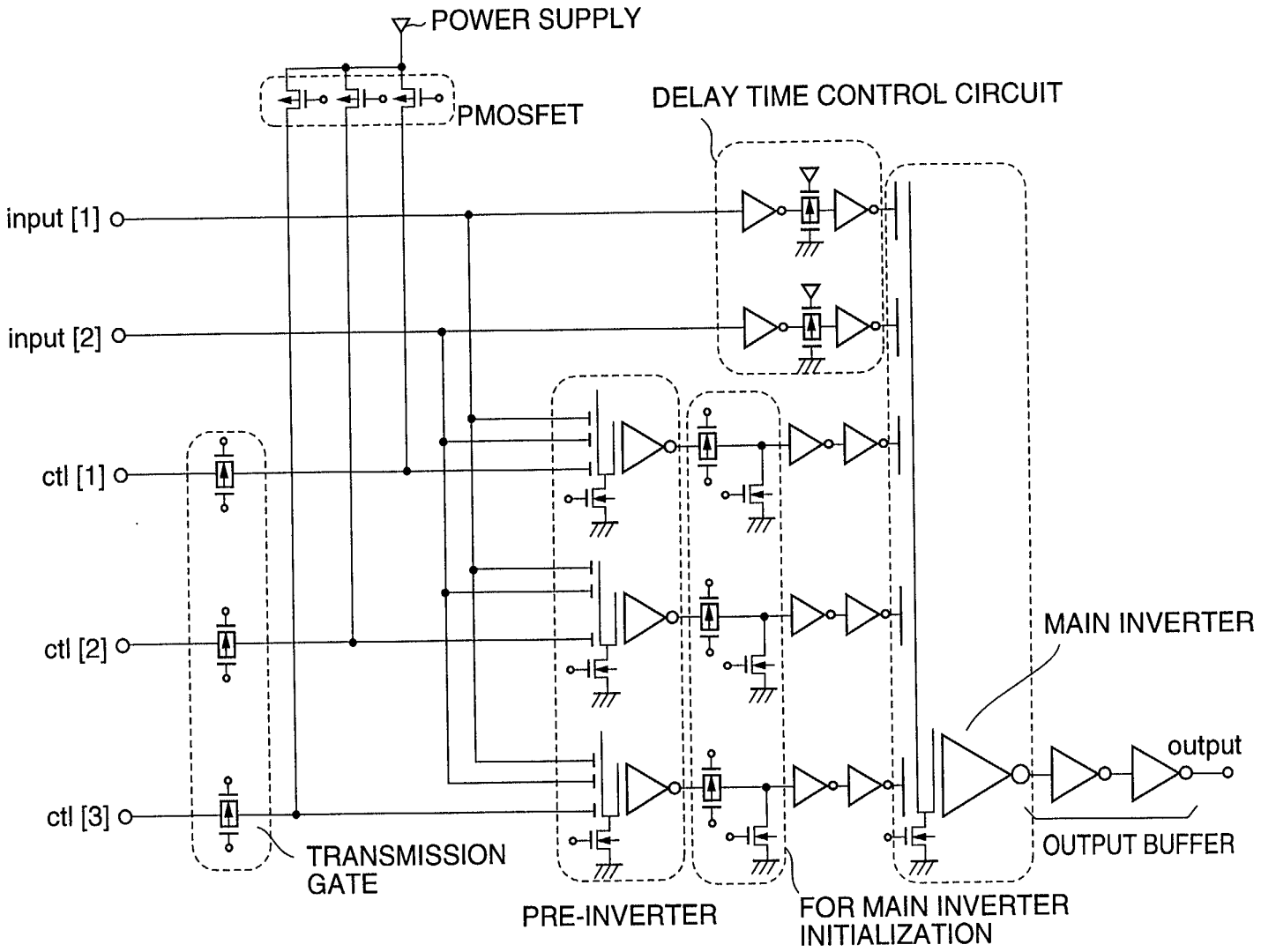


FIG.53

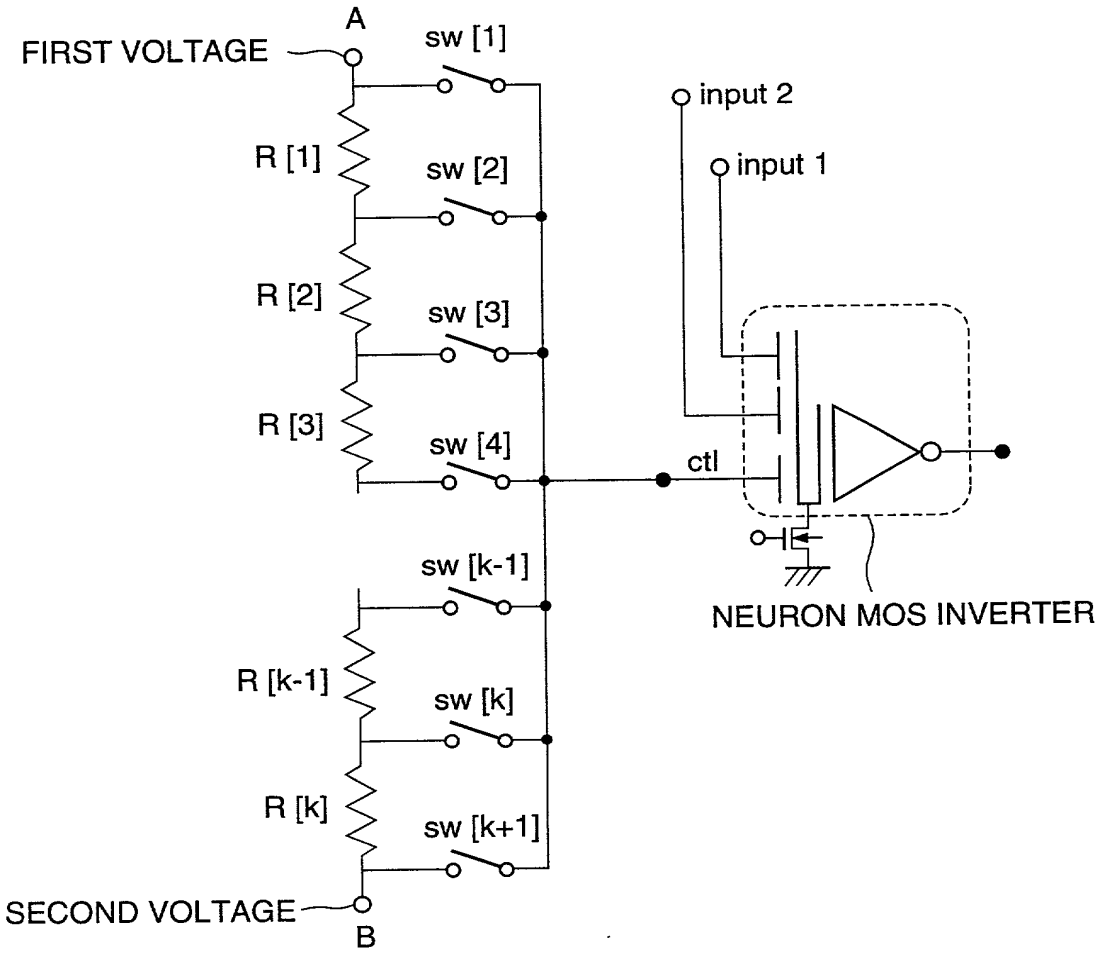

A
FIRST VOLTAGE
sw [1]
input 2
input 1
R [1]
sw [2]
R [2]
sw [3]
R [3]
sw [4]
ctl
sw [k-1]
R [k-1]
sw [k]
R [k]
sw [k+1]
SECOND VOLTAGE
B
NEURON MOS INVERTER

FIG.54

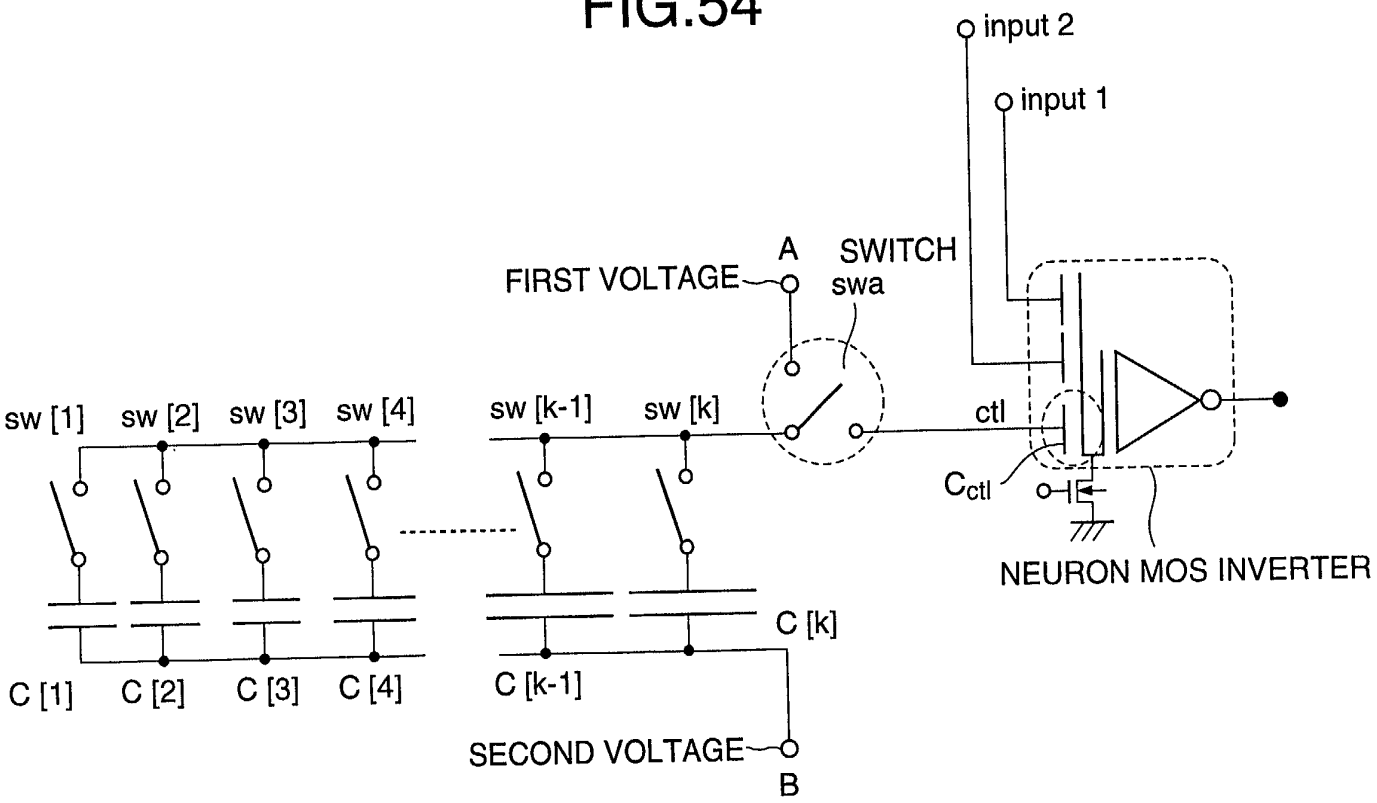


FIG.55

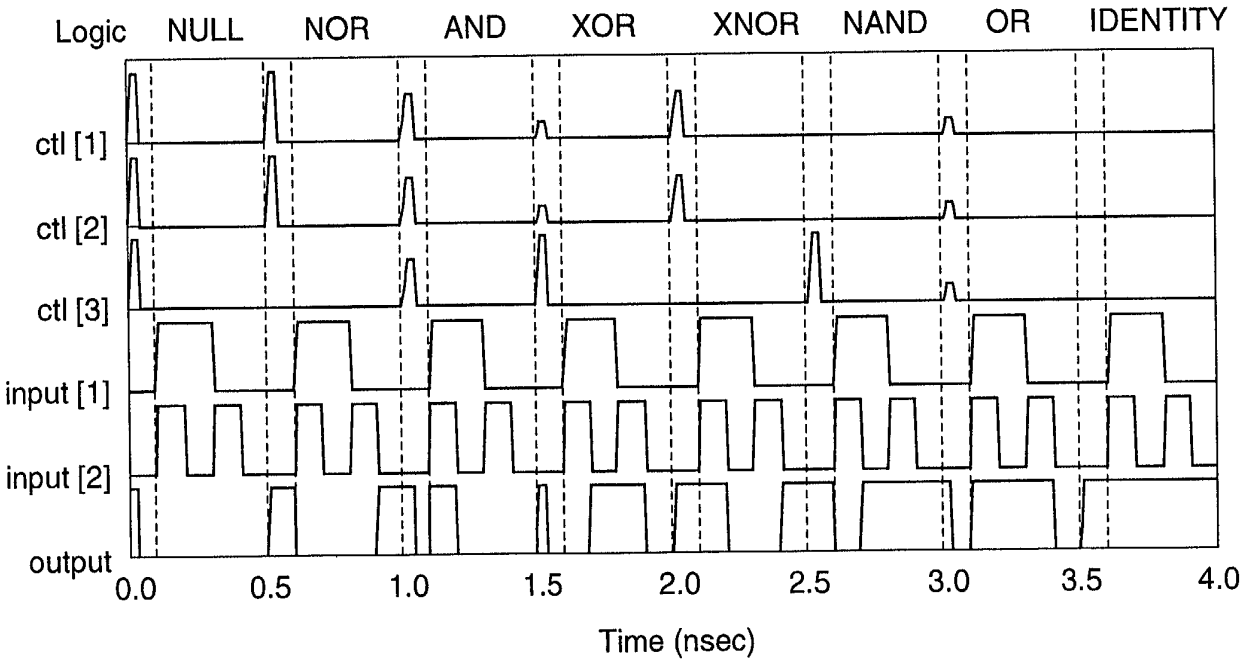


FIG.56

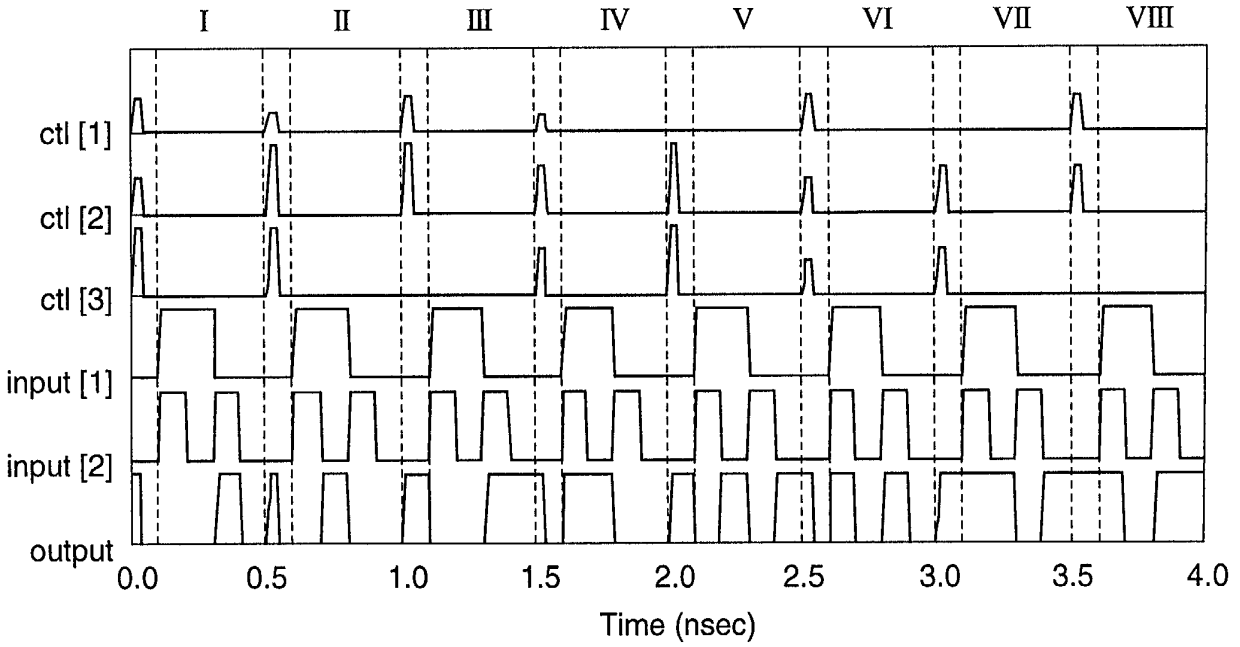

I
II
III
IV
V
VI
VII
VIII
ctl [1]
ctl [2]
ctl [3]
input [1]
input [2]
output
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Time (nsec)

FIG.57

INTERVAL	I	II	III	IV	V	VI	VII	VIII
LOGIC FORMULA	$X'_1 \cdot X_2$	$X_1 \cdot X'_2$	X'_1	X_1	X'_2	X_2	$X_1 + X'_2$	$X'_1 + X'_2$

FIG.58

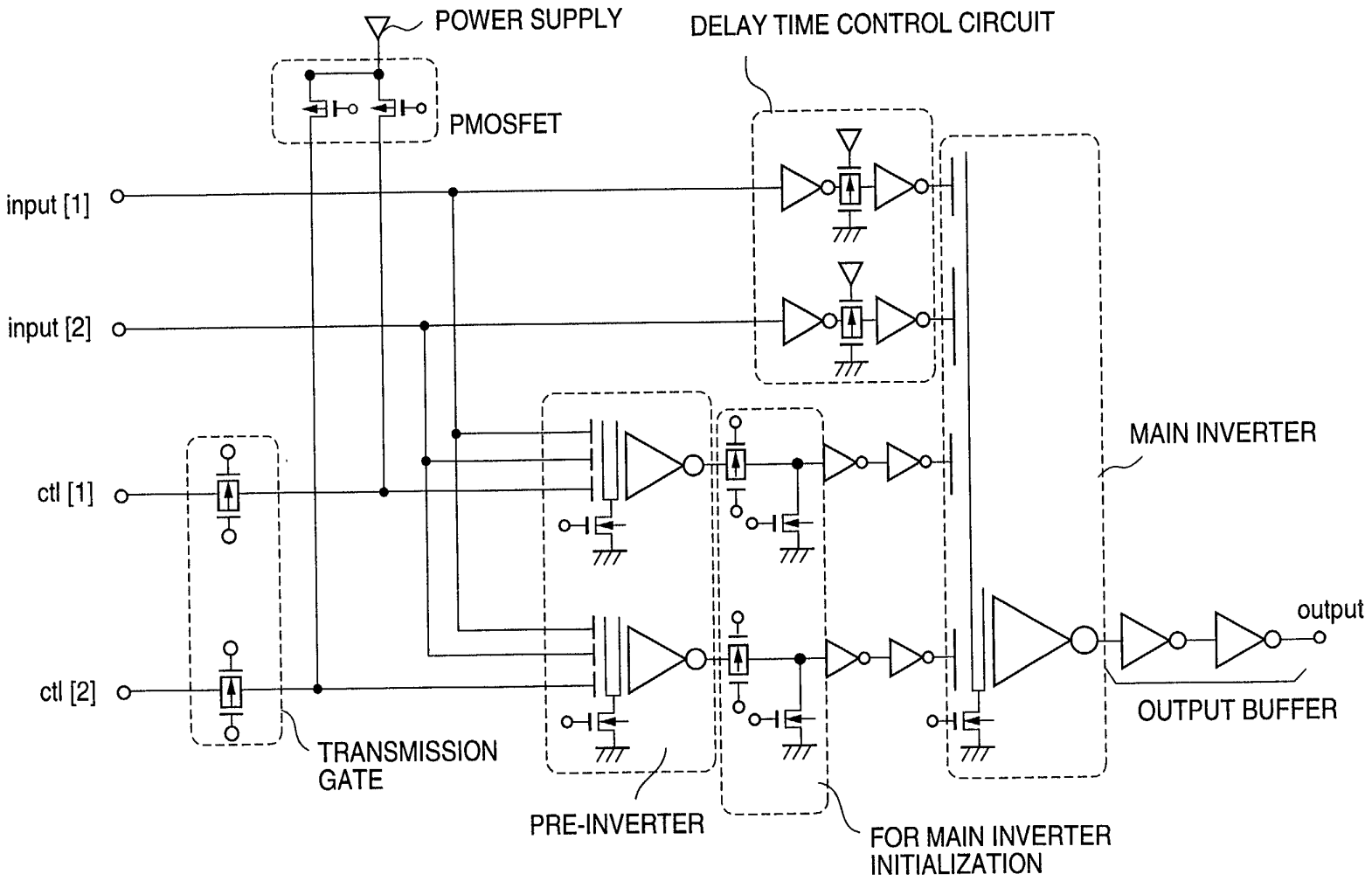


FIG.59

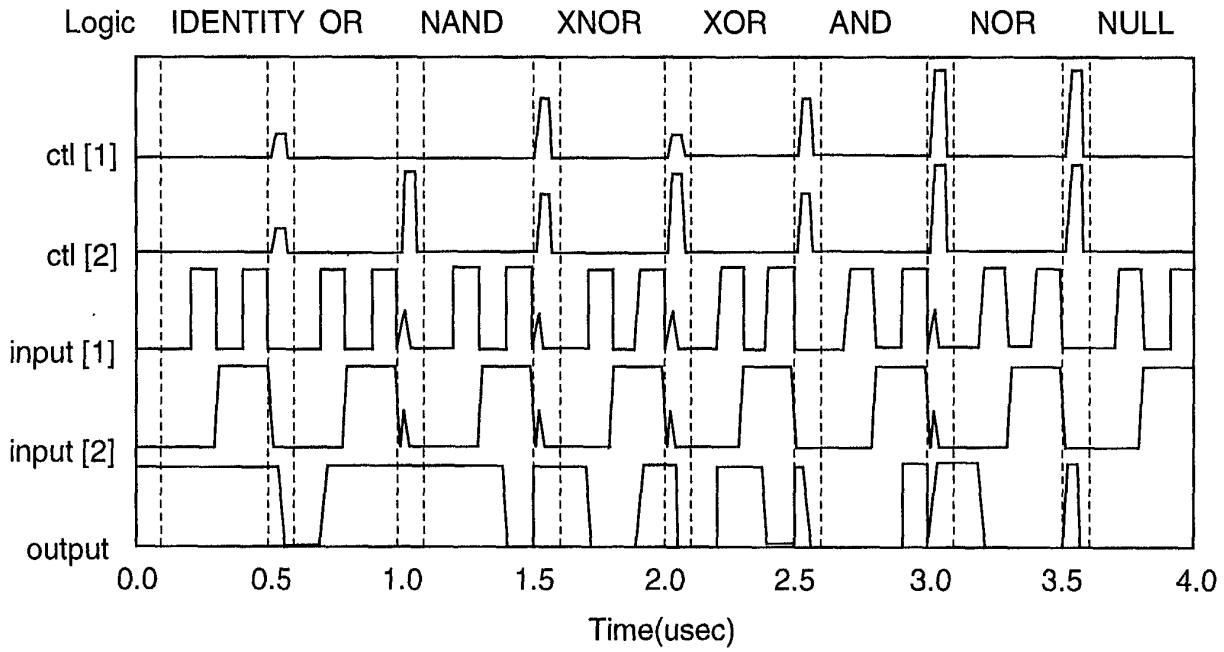


FIG.60

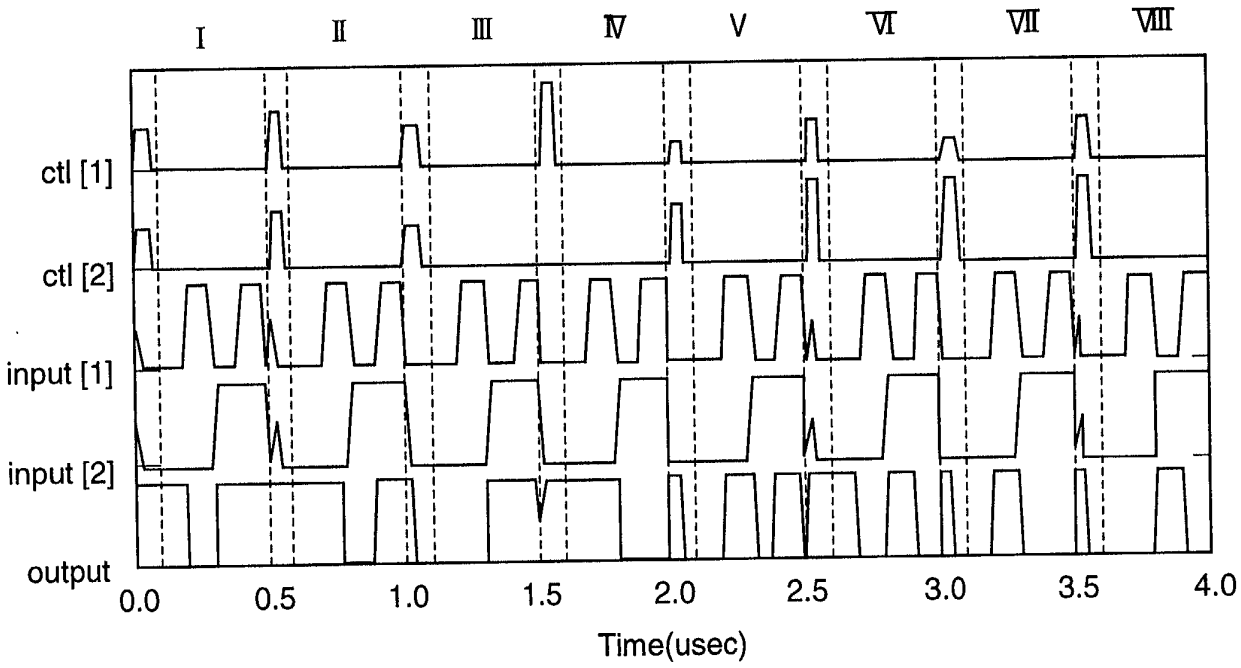


FIG.61

INTERVAL	I	II	III	IV	V	VI	VII	VIII
LOGIC FORMULA	X'_1+X_2	$X_1+X'_2$	X_2	X'_2	X_1	X'_1	$X_1 \cdot X'_2$	$X'_1 \cdot X'_2$

FIG.62A

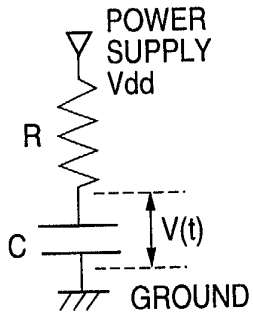


FIG.62B

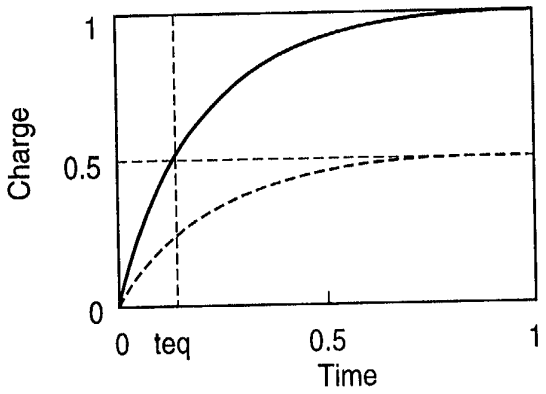


FIG.62C

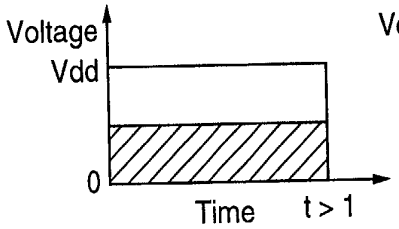


FIG.62D

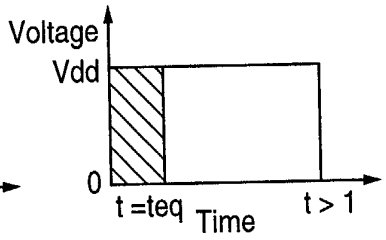


FIG.63A

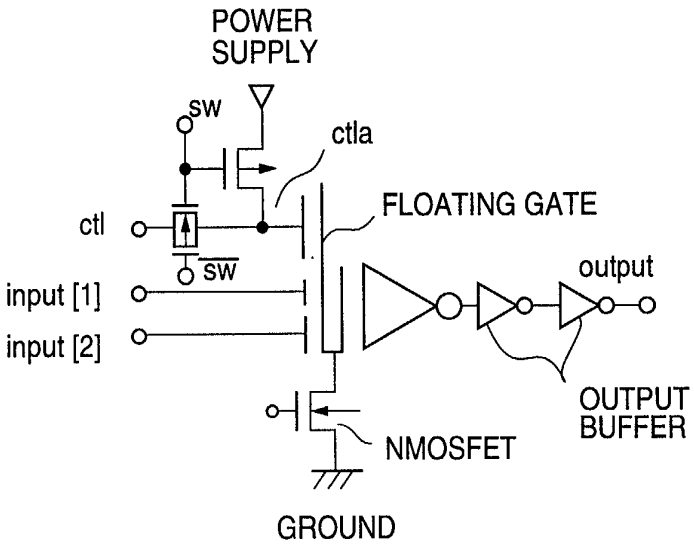


FIG.63B

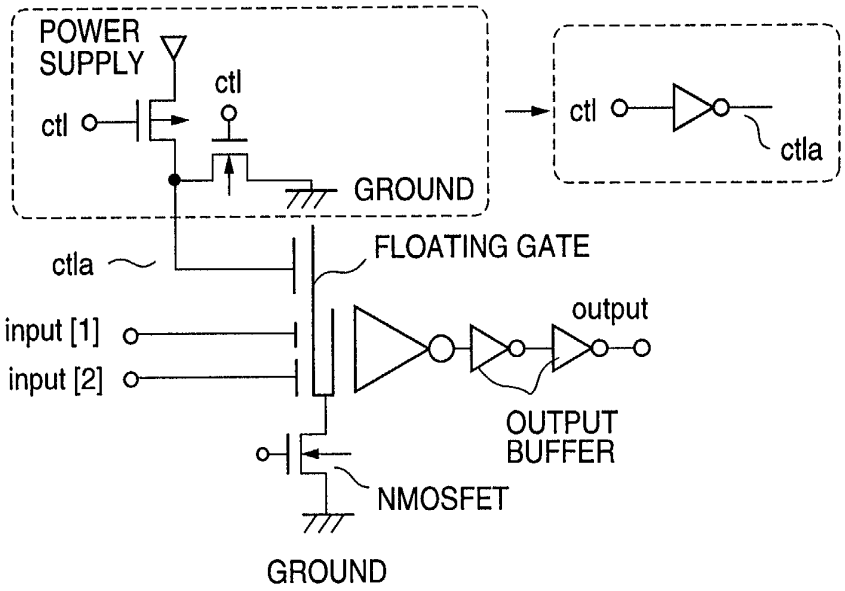


FIG.64

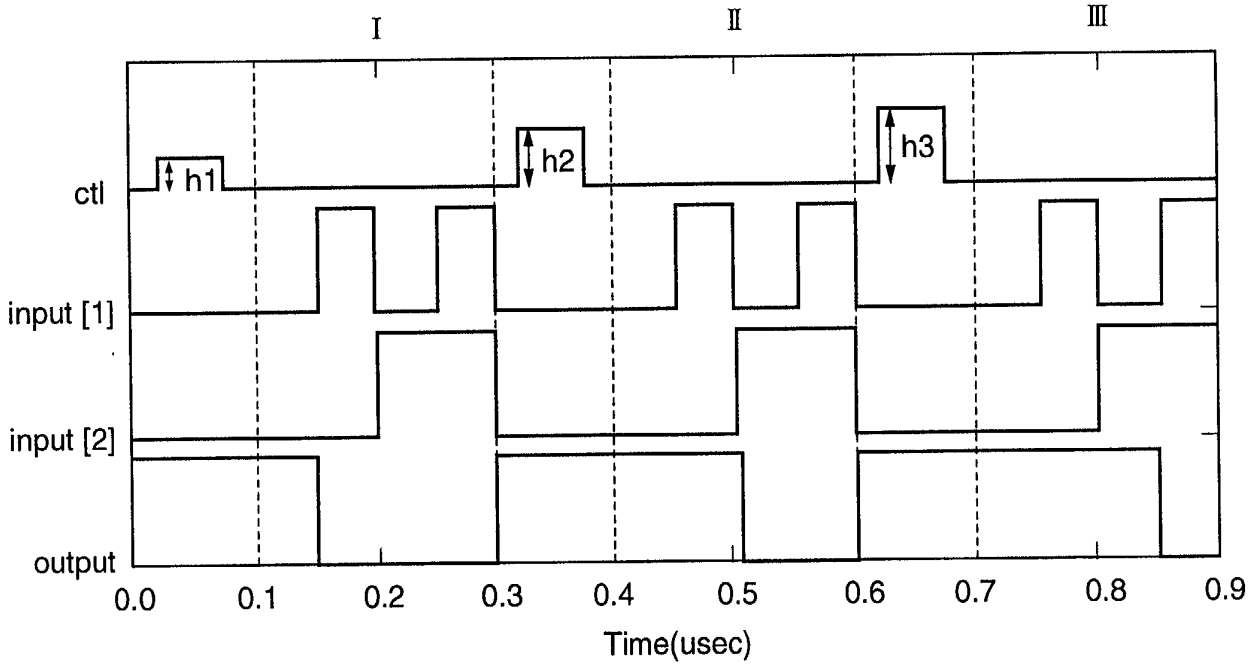


FIG.65

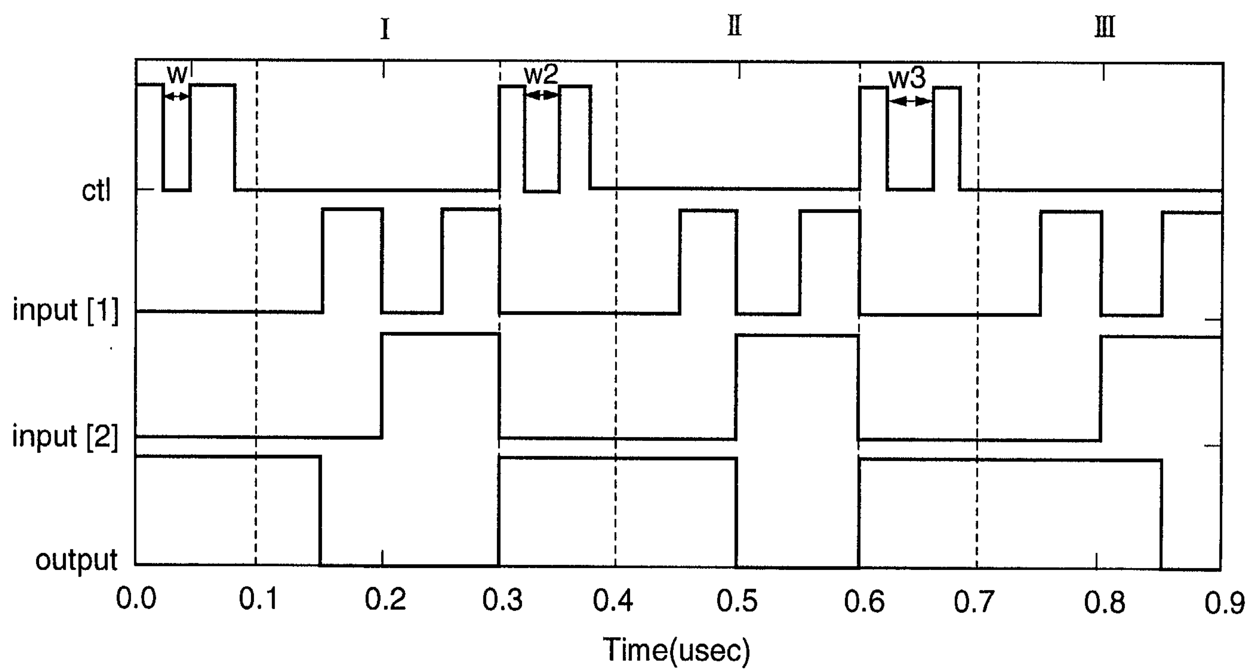


FIG.66

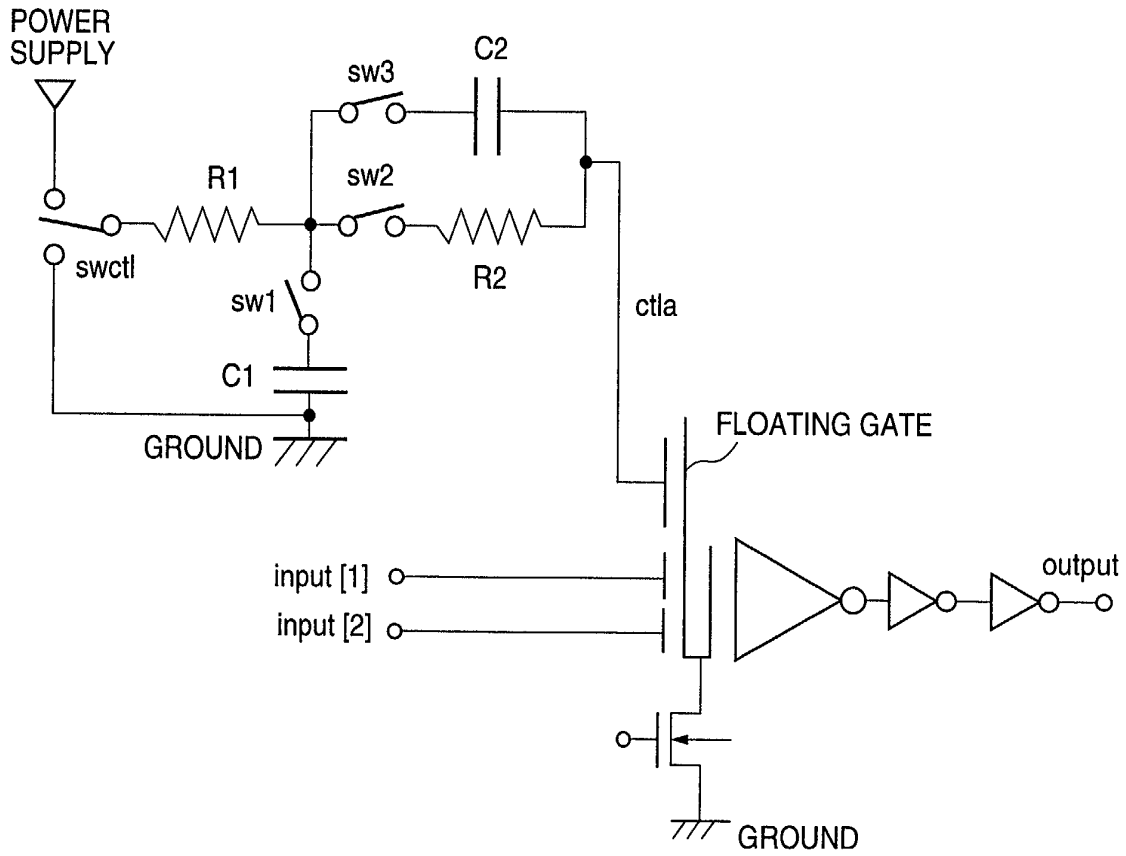

POWER SUPPLY
C2
sw3
R1
sw2
swctl
R2
sw1
ctla
C1
GROUND
FLOATING GATE
input [1]
input [2]
output
GROUND

FIG.67

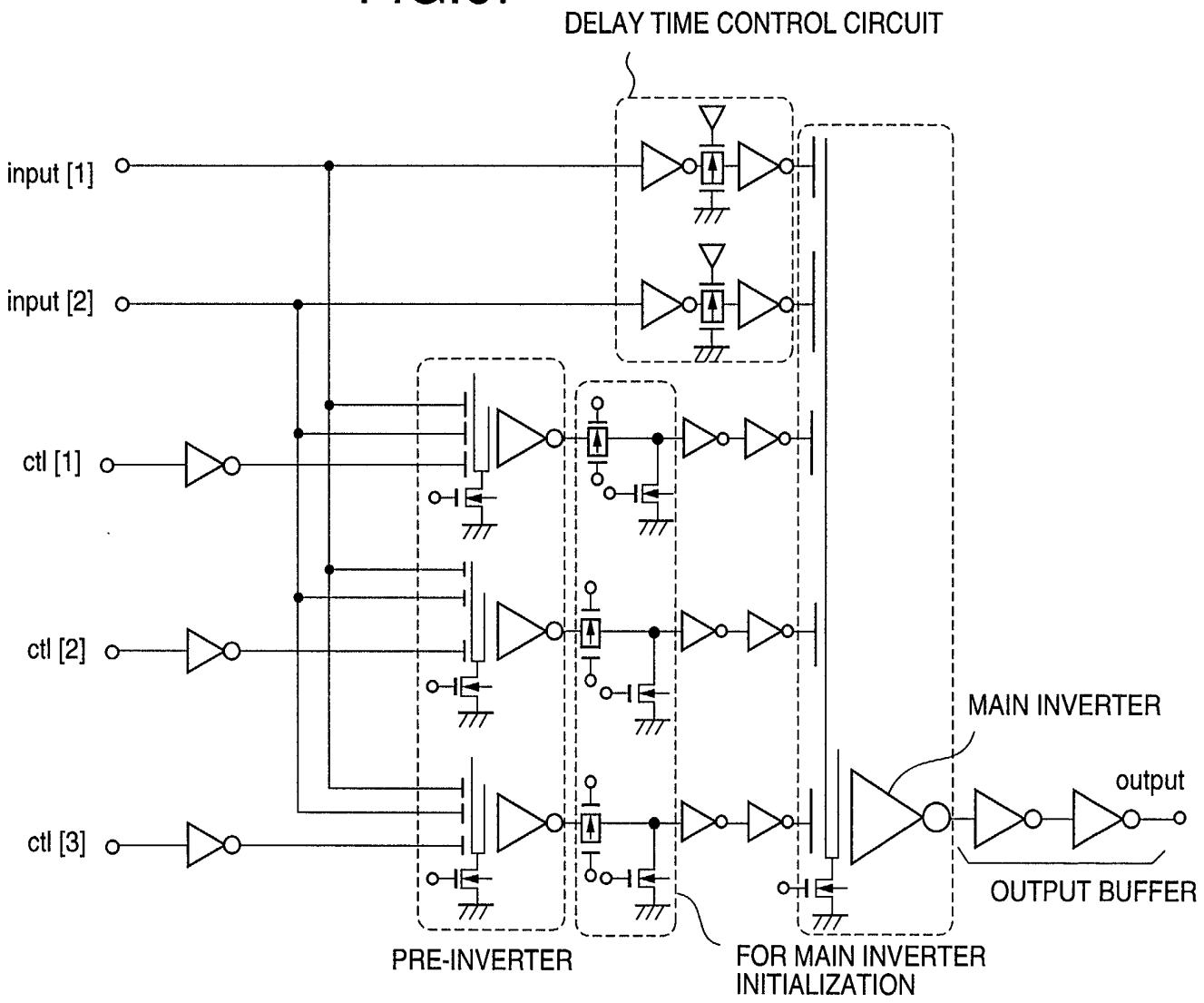

DELAY TIME CONTROL CIRCUIT
input [1]
input [2]
ctl [1]
ctl [2]
ctl [3]
MAIN INVERTER
output
OUTPUT BUFFER
PRE-INVERTER
FOR MAIN INVERTER INITIALIZATION

FIG.68

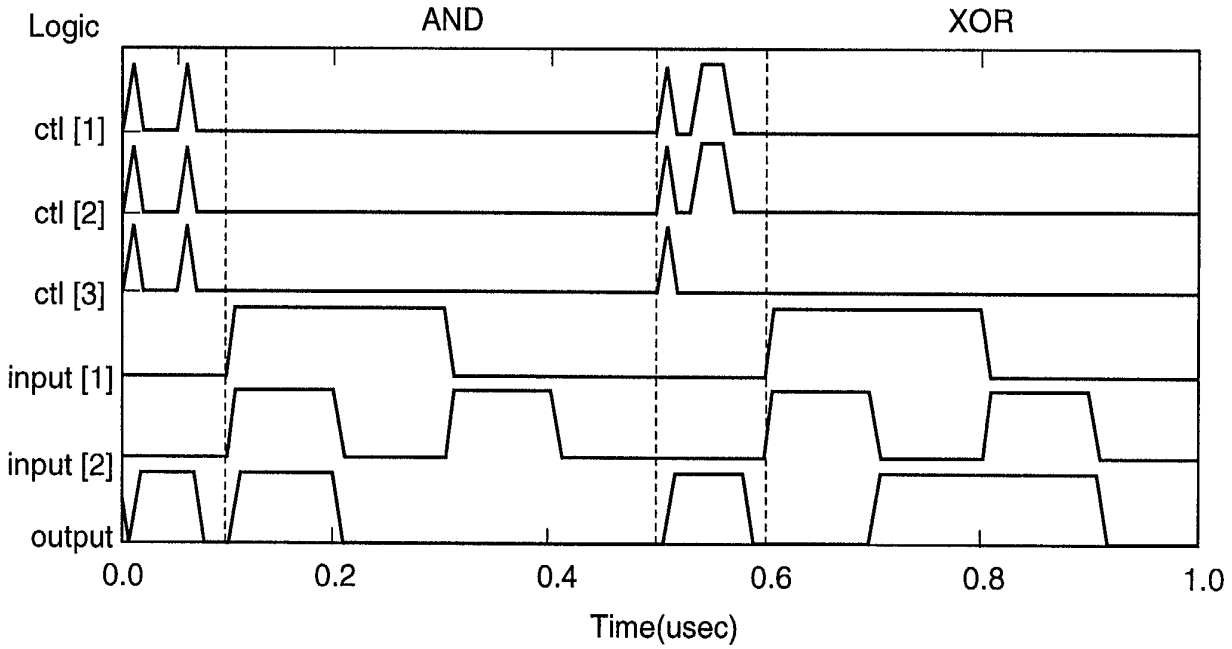


FIG.69

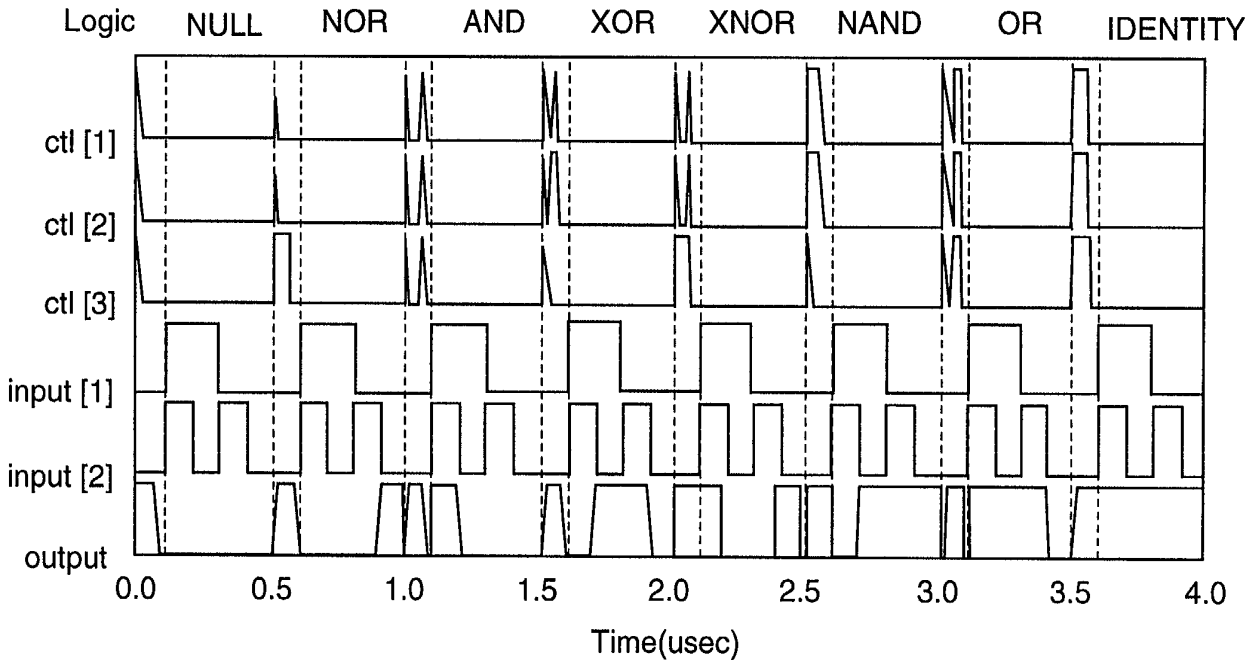

Logic
NULL
NOR
AND
XOR
XNOR
NAND
OR
IDENTITY
ctl [1]
ctl [2]
ctl [3]
input [1]
input [2]
output
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Time(usec)

FIG.70

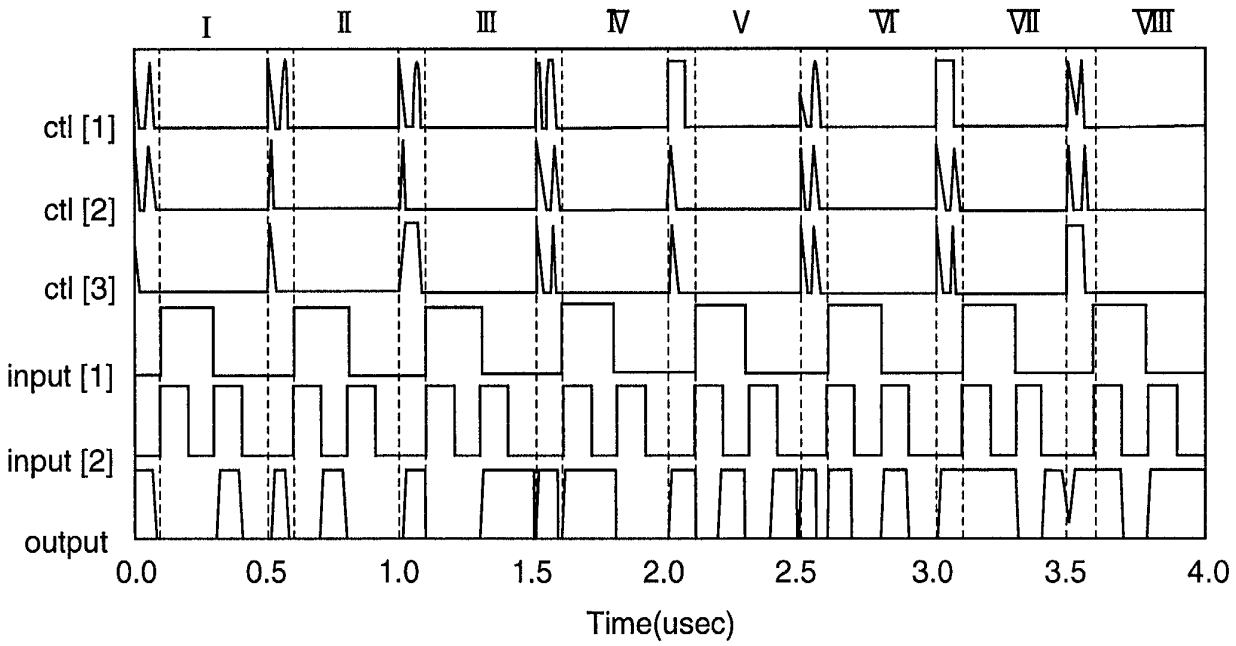


FIG.71

INTERVAL	I	II	III	IV	V	VI	VII	VIII
LOGIC FORMULA	$X'_1 \cdot X_2$	$X_1 \cdot X'_2$	X'_1	X_1	X'_2	X_2	$X_1+X'_2$	X'_1+X_2

FIG.72A

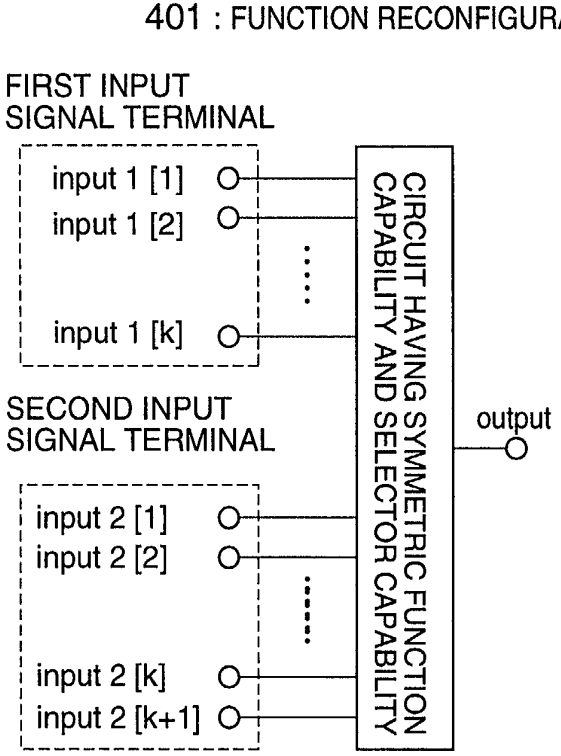


FIG.72B

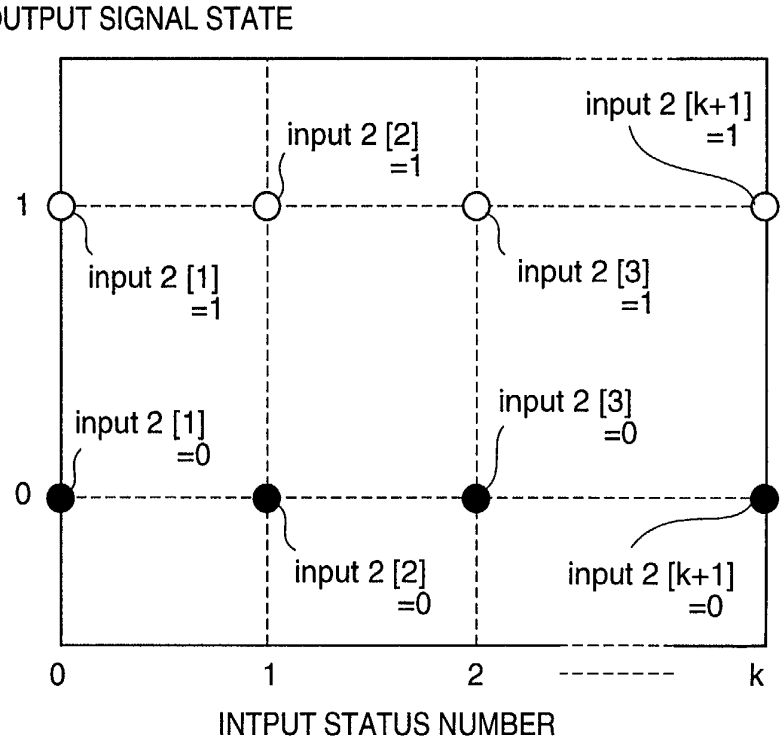


FIG.73

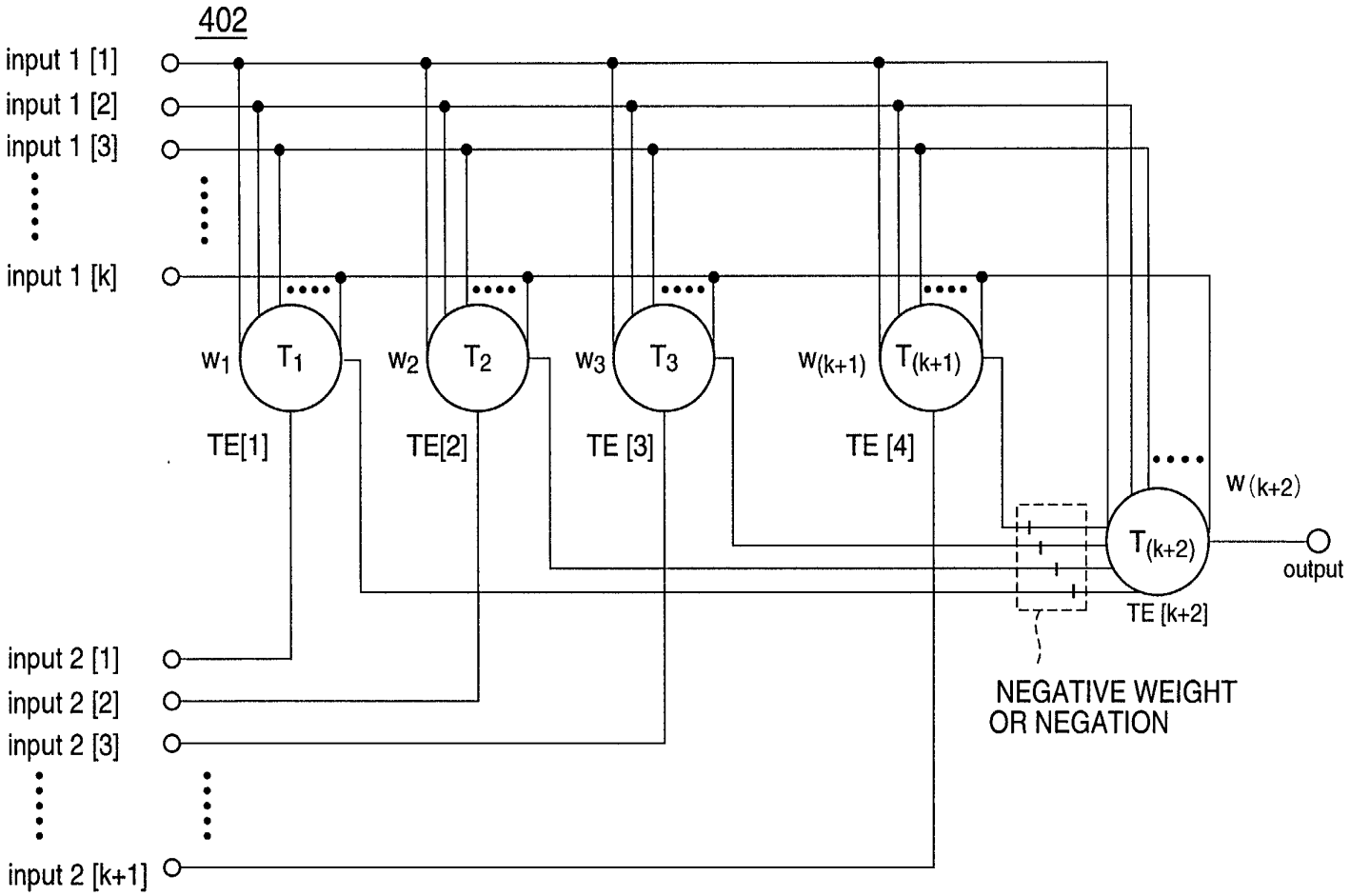


FIG.74

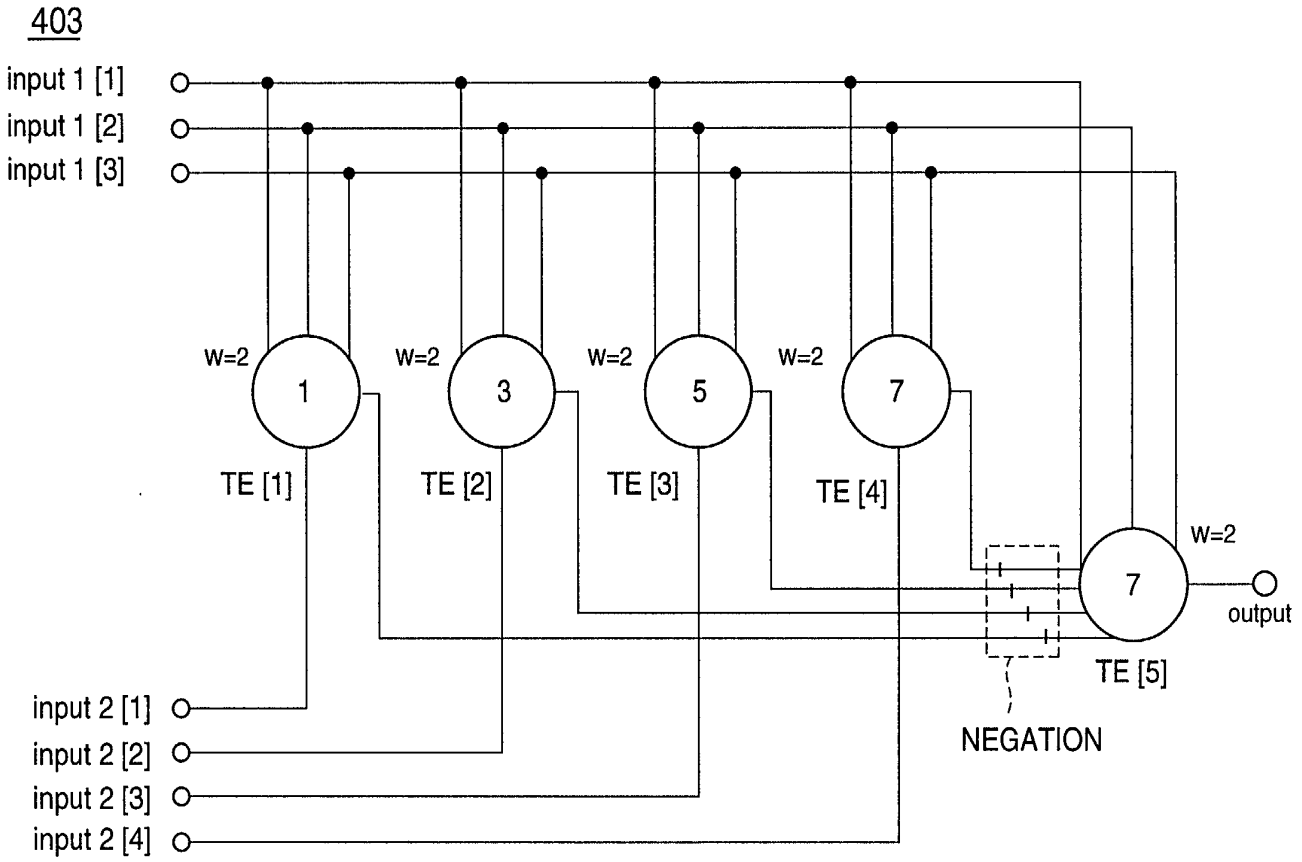

403
input 1 [1]
input 1 [2]
input 1 [3]
W=2
1
W=2
3
W=2
5
W=2
7
TE [1]
TE [2]
TE [3]
TE [4]
W=2
7
output
TE [5]
NEGATION
input 2 [1]
input 2 [2]
input 2 [3]
input 2 [4]

FIG.75

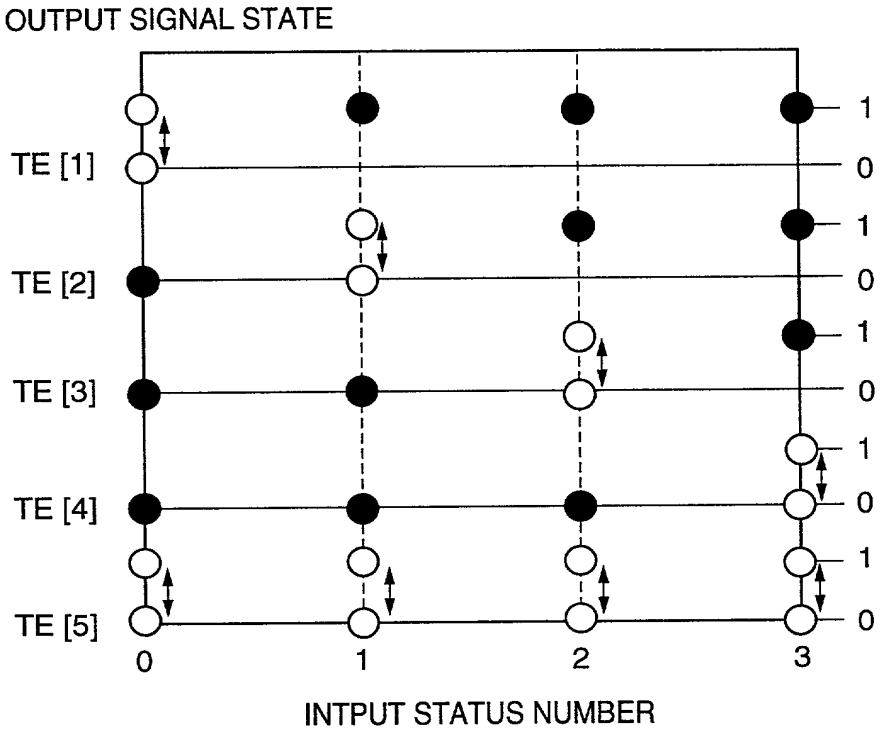

OUTPUT SIGNAL STATE
TE [1]
TE [2]
TE [3]
TE [4]
TE [5]
1
0
1
0
1
0
1
0
1
0
0
1
2
3
INTPUT STATUS NUMBER

FIG.76A

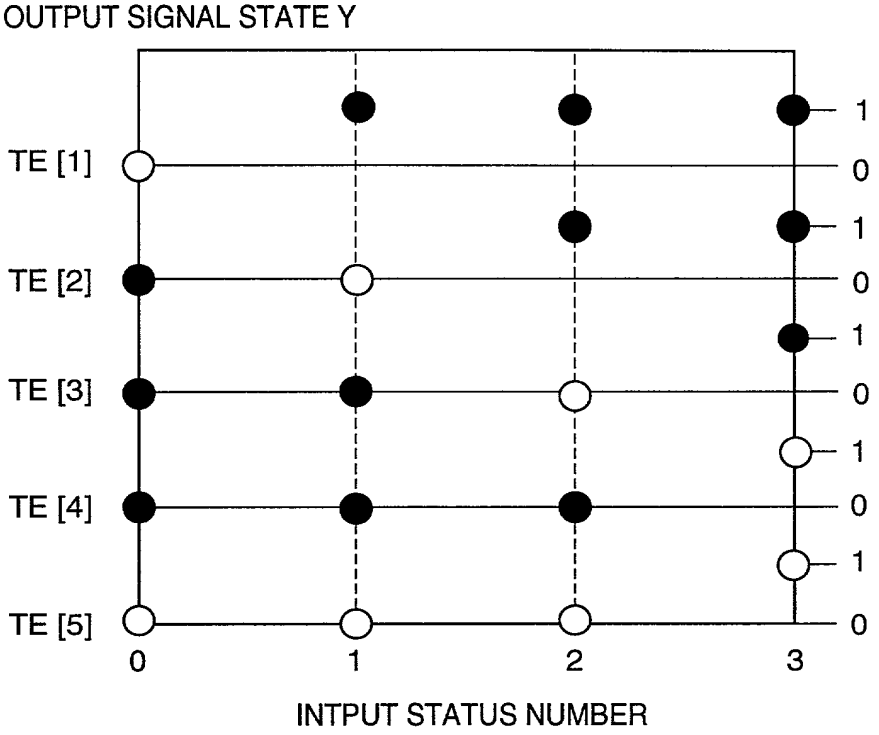


FIG.76B

m	X_1	X_2	X_3	Y
0	0	0	0	0
1	0	0	1	0
	0	1	0	0
	1	0	0	0
2	0	1	1	0
	1	0	1	0
	1	1	0	0
3	1	1	1	1

FIG.77

404 : FUNCTION RECONFIGURABLE INTEGRATED CIRCUIT

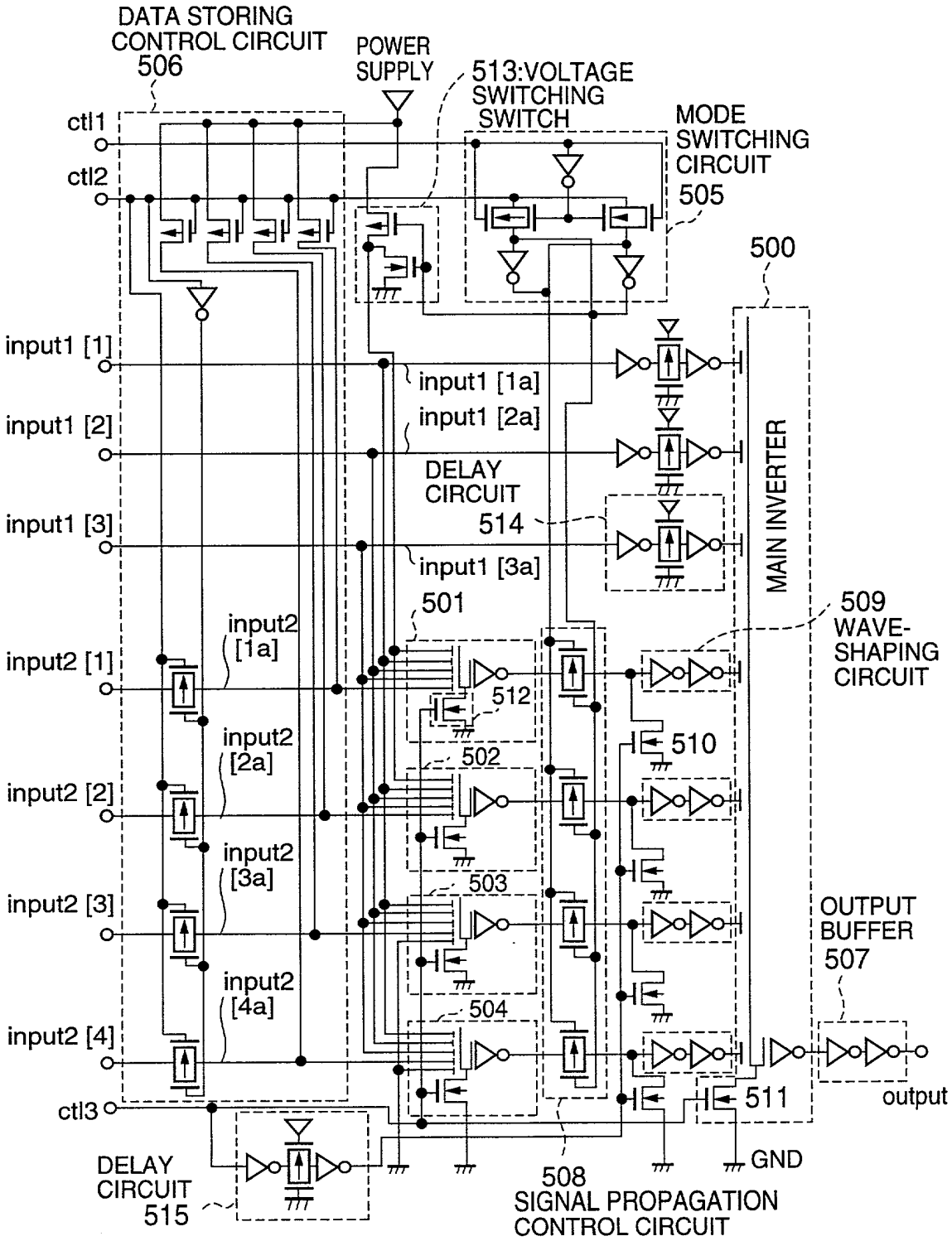


FIG.78

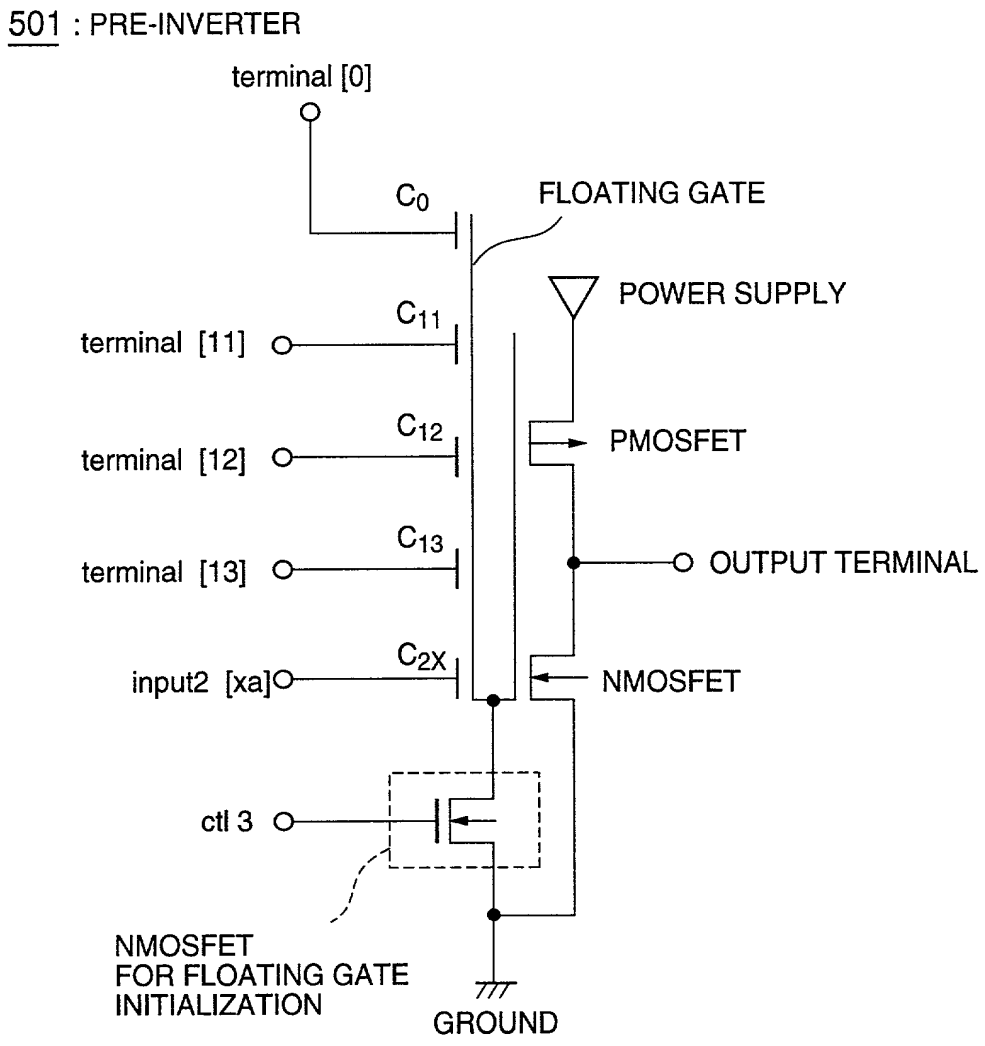

501 : PRE-INVERTER
terminal [0]
C0
FLOATING GATE
POWER SUPPLY
C11
terminal [11]
C12
terminal [12]
PMOSFET
C13
terminal [13]
OUTPUT TERMINAL
C2X
input2 [xa]
NMOSFET
ctl 3
NMOSFET
FOR FLOATING GATE
INITIALIZATION
GROUND

FIG.79

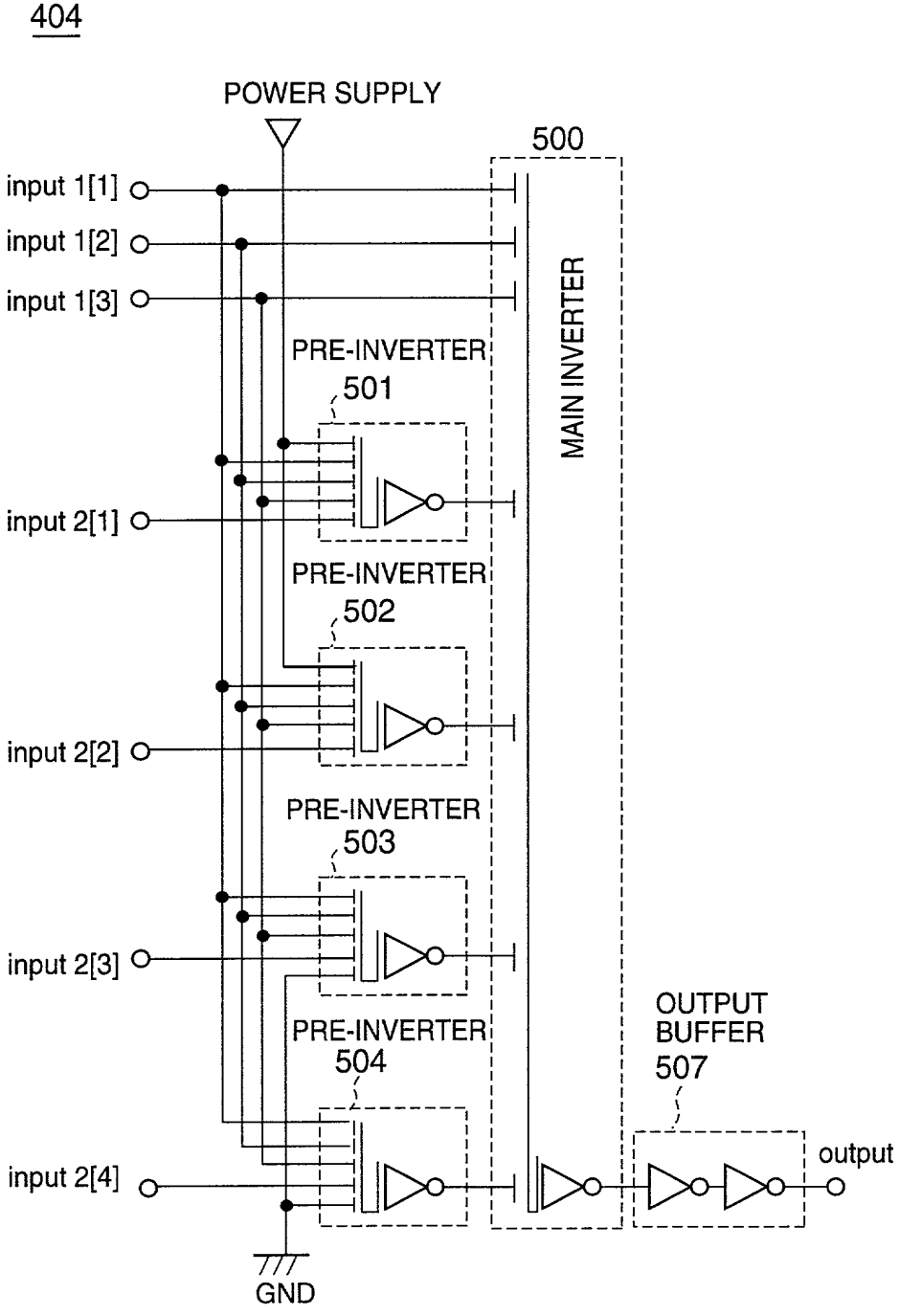

404
POWER SUPPLY
500
input 1[1]
input 1[2]
input 1[3]
PRE-INVERTER
501
MAIN INVERTER
input 2[1]
PRE-INVERTER
502
input 2[2]
PRE-INVERTER
503
input 2[3]
OUTPUT
BUFFER
507
PRE-INVERTER
504
output
input 2[4]
GND

FIG.80

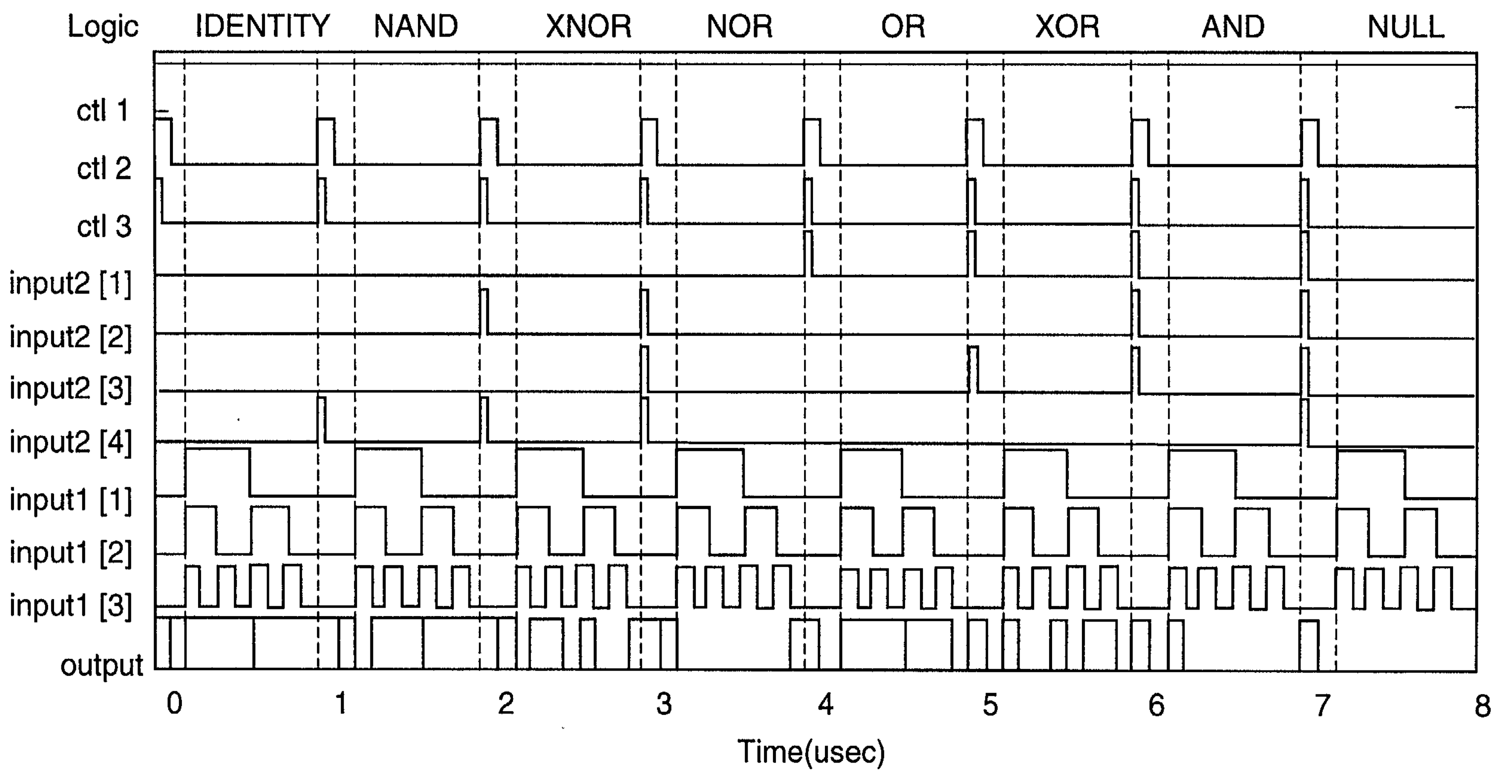
TERMINAL NAME	TERMINAL VOLTAGE DURING INITIALIZATION TIME				TERMINAL VOLTAGE DURING FUNCTION PROCESSING
	1	2	3	4	
ctl1	Vdd	→	→	→	Vdd
ctl2	Vdd	→	→	0	0
ctl3	Vdd	→	0	⇢	0
input 1	0	⇢	⇢	⇢	Vsig
input 2	0	V'conf	→	→	——

V'conf : VOLTAGE OF LOGICAL INVERSION OF FUNCTION CONFIGURATION DATA
Vsig : INPUT SIGNAL VOLTAGE DURING FUNCTION PROCESSING

FIG.81

TERMINAL NAME	TERMINAL VOLTAGE DURING INITIALIZATION TIME			TERMINAL VOLTAGE DURING PERFORMING SELECTOR CAPABILITY
	1	2	3	
ctl1	Vdd	→	0	0
ctl2	Vdd	→	→	Vdd
ctl3	Vdd	0	⇢	0
input 1	0	⇢	⇢	CONTROL INPUT SIGNAL VOLTAGE
input 2	0	⇢	⇢	DATA INPUT SIGNAL VOLTAGE

FIG.82



Logic
IDENTITY
NAND
XNOR
NOR
OR
XOR
AND
NULL
ctl 1
ctl 2
ctl 3
input2 [1]
input2 [2]
input2 [3]
input2 [4]
input1 [1]
input1 [2]
input1 [3]
output
0
1
2
3
4
5
6
7
8
Time(usec)

FIG.83

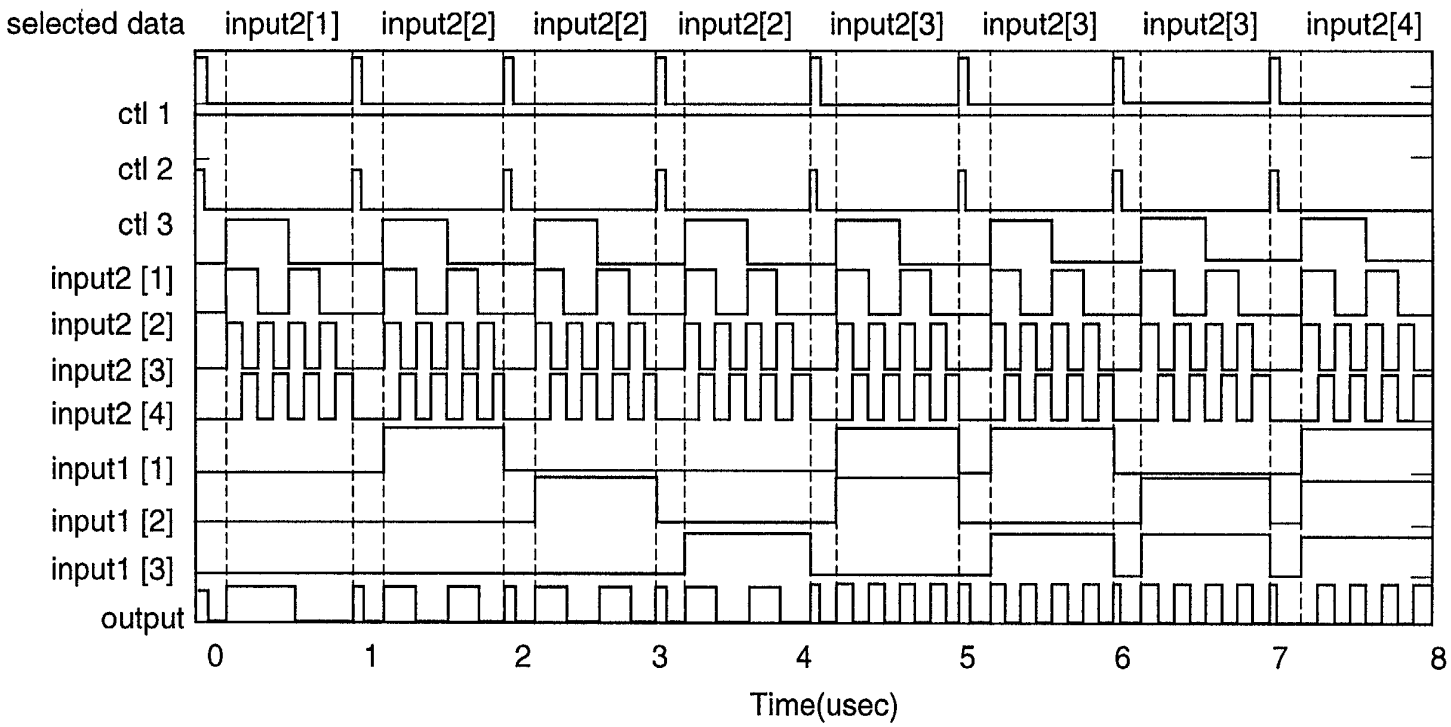

selected data
input2[1]
input2[2]
input2[2]
input2[2]
input2[3]
input2[3]
input2[3]
input2[4]
ctl 1
ctl 2
ctl 3
input2 [1]
input2 [2]
input2 [3]
input2 [4]
input1 [1]
input1 [2]
input1 [3]
output
0
1
2
3
4
5
6
7
8
Time(usec)

FIG.84

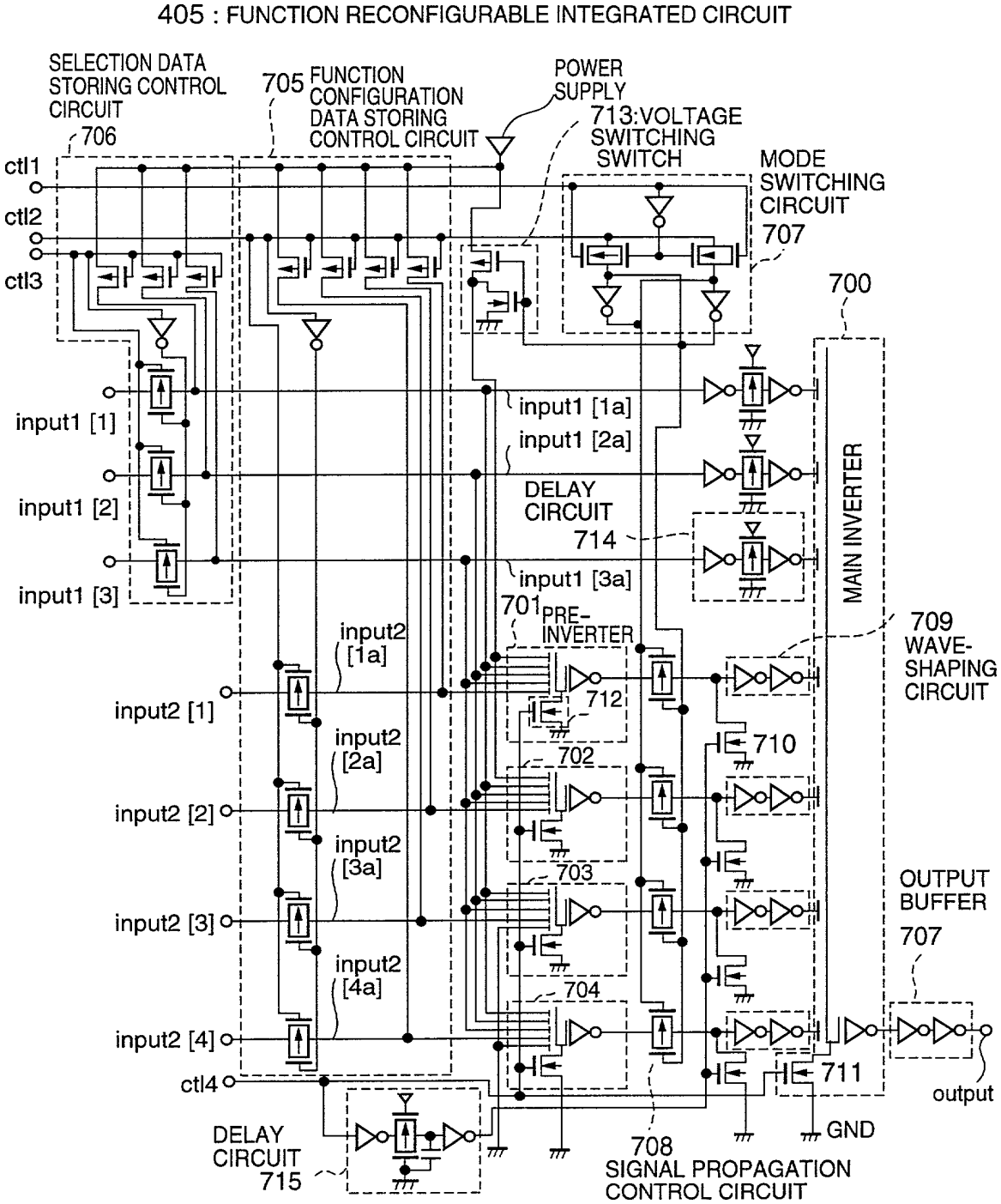

405 : FUNCTION RECONFIGURABLE INTEGRATED CIRCUIT
SELECTION DATA STORING CONTROL CIRCUIT
706
705 FUNCTION CONFIGURATION DATA STORING CONTROL CIRCUIT
POWER SUPPLY
713:VOLTAGE SWITCHING SWITCH
MODE SWITCHING CIRCUIT
707
700
ctl1
ctl2
ctl3
input1 [1]
input1 [2]
input1 [3]
input1 [1a]
input1 [2a]
input1 [3a]
DELAY CIRCUIT
714
MAIN INVERTER
701
PRE-INVERTER
709
WAVE-SHAPING CIRCUIT
input2 [1]
input2 [2]
input2 [3]
input2 [4]
input2 [1a]
input2 [2a]
input2 [3a]
input2 [4a]
712
710
702
703
704
OUTPUT BUFFER
707
output
ctl4
711
GND
DELAY CIRCUIT
715
708
SIGNAL PROPAGATION CONTROL CIRCUIT

FIG.85

601 : NEURON MOS INVERTER HAVING A SWITCH

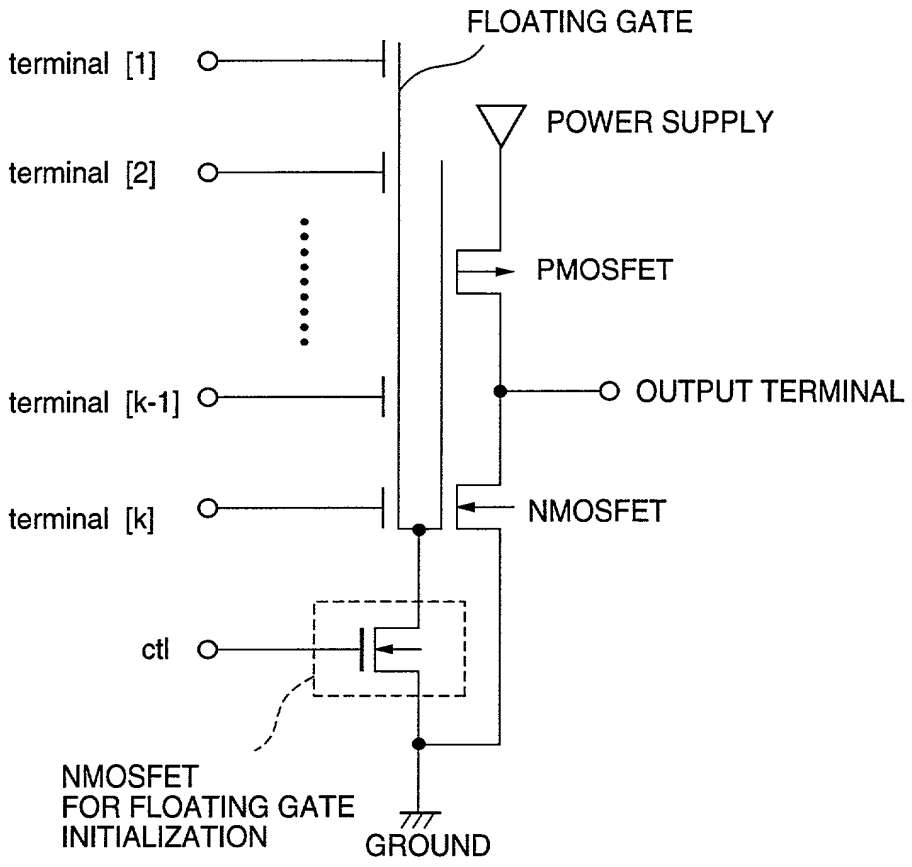


FIG.86

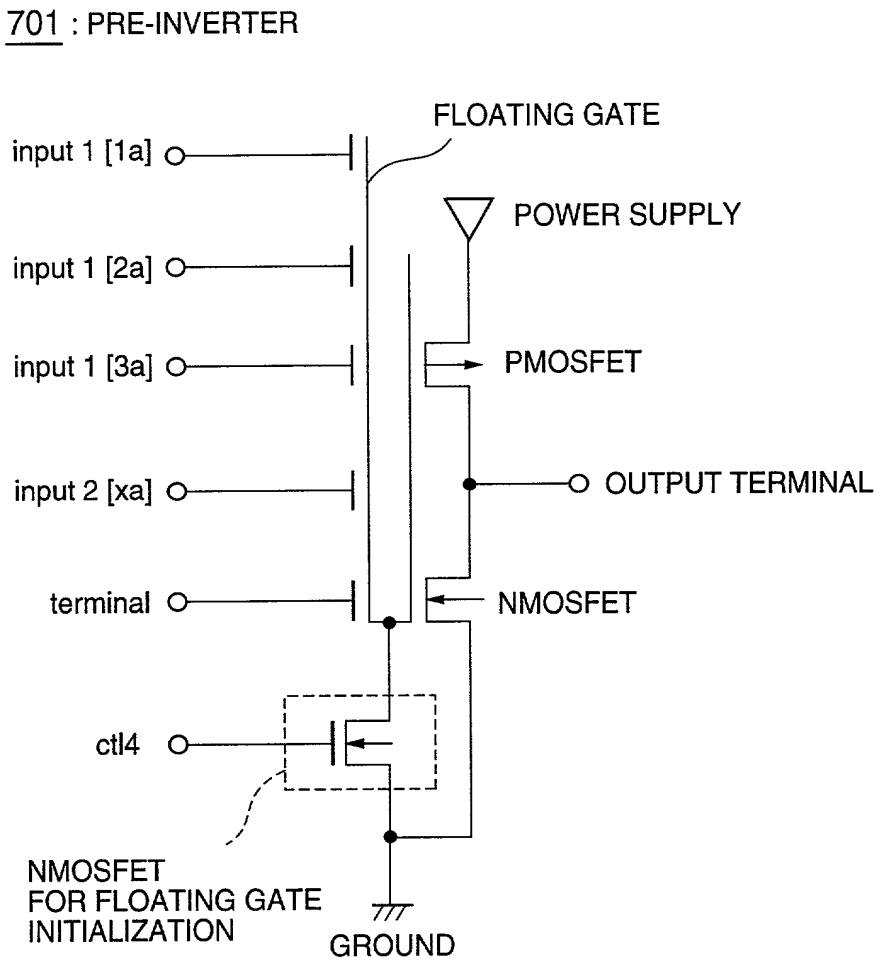

701 : PRE-INVERTER
FLOATING GATE
input 1 [1a]
POWER SUPPLY
input 1 [2a]
input 1 [3a]
PMOSFET
input 2 [xa]
OUTPUT TERMINAL
terminal
NMOSFET
ctl4
NMOSFET
FOR FLOATING GATE
INITIALIZATION
GROUND

FIG.87

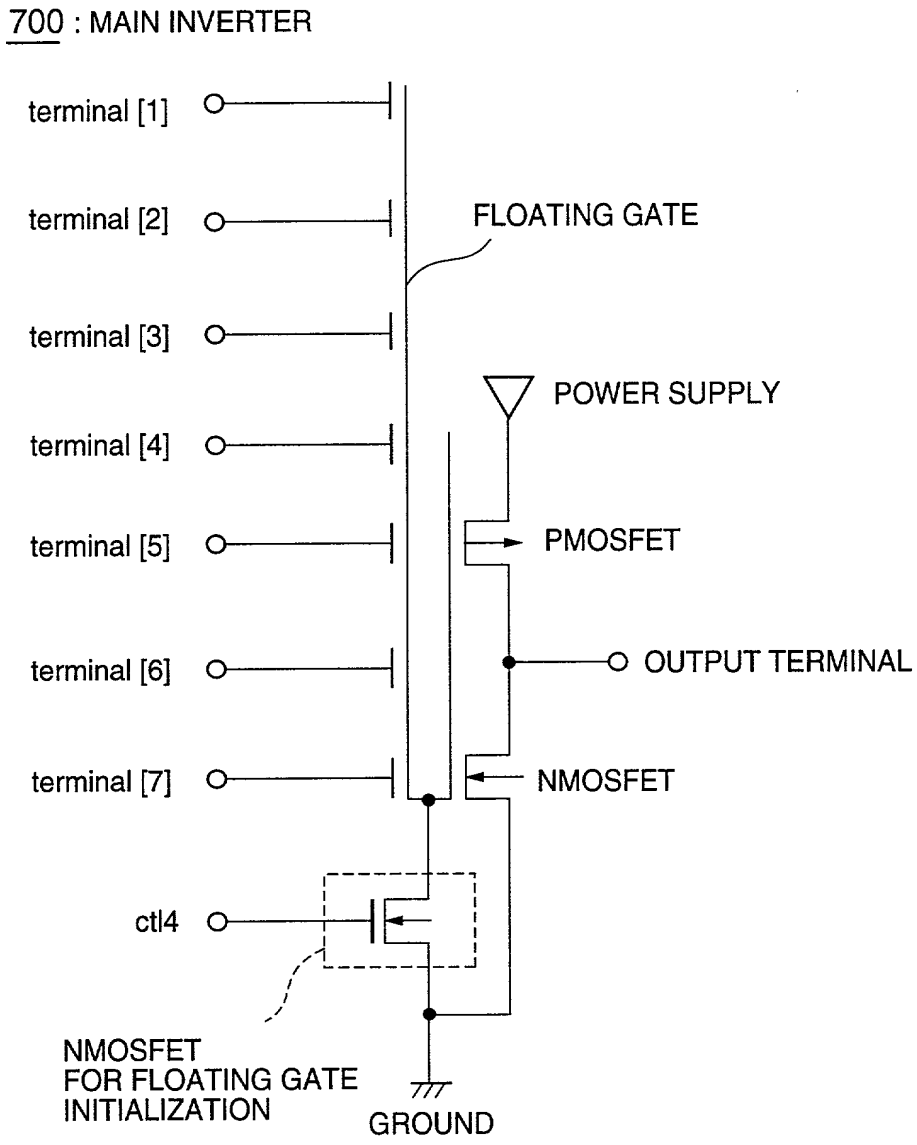

700 : MAIN INVERTER
terminal [1]
terminal [2]
terminal [3]
terminal [4]
terminal [5]
terminal [6]
terminal [7]
FLOATING GATE
POWER SUPPLY
PMOSFET
OUTPUT TERMINAL
NMOSFET
ctl4
NMOSFET
FOR FLOATING GATE
INITIALIZATION
GROUND

FIG.88

TERMINAL NAME	TERMINAL VOLTAGE DURING INITIALIZATION TIME			TERMINAL VOLTAGE DURING FUNCTION PROCESSING
	1	2	3	
ctl1	Vdd	——→	0	0
ctl2	Vdd	——→	——→	Vdd
ctl3	Vdd	——→	——→	Vdd
ctl4	Vdd	0	- - - →	0
input 1	0	- - - →	- - - →	Vsig
input 2	0	- - - →	- - - →	Vconf

Vconf : VOLTAGE OF FUNCTION CONFIGURATION DATA
Vsig : INPUT SIGNAL VOLTAGE DURING FUNCTION PROCESSING

FIG.89

TERMINAL NAME	TERMINAL VOLTAGE DURING INITIALIZATION TIME			TERMINAL VOLTAGE DURING FUNCTION PROCESSING
	1	2	3	
ctl1	Vdd	——→	——→	Vdd
ctl2	Vdd	Vdd	0	0
ctl3	Vdd	——→	——→	Vdd
ctl4	Vdd	0	- - - →	0
input 1	0	- - - →	- - - →	Vsig
input 2	V'conf	V'conf	V'conf	——

V'conf : VOLTAGE OF LOGICAL INVERSION OF FUNCTION CONFIGURATION DATA
Vsig : INPUT SIGNAL VOLTAGE DURING FUNCTION PROCESSING

FIG.90

TERMINAL NAME	TERMINAL VOLTAGE DURING INITIALIZATION TIME			TERMINAL VOLTAGE DURING PERFOMING SELECTOR CAPABILTY
	1	2	3	
ctl1	Vdd	→	0	0
ctl2	Vdd	→	→	Vdd
ctl3	Vdd	→	→	Vdd
ctl4	Vdd	0	---→	0
input 1	0	---→	---→	Vsel
input 2	0	---→	---→	Vdata

Vsel : VOLTAGE OF ADDRESS SIGNAL OF DATA TO BE SELECTED
Vdata : INPUT SIGNAL VOLTAGE OF DATA TO BE SELECTED

FIG.91

TERMINAL NAME	TERMINAL VOLTAGE DURING INITIALIZATION TIME					TERMINAL VOLTAGE DURING PERFOMING SELECTOR CAPABILTY
	1	2	3	4	5	
ctl1	Vdd	→	→	→	0	0
ctl2	Vdd	→	→	→	→	Vdd
ctl3	Vdd	→	0	---→	---→	0
ctl4	Vdd	0	---→	---→	---→	0
input 1	V'sel	V'sel	V'sel	0	---→	——
input 2	0	---→	---→	---→	---→	Vdata

V'sel : VOLTAGE OF LOGICAL INVERSION OF ADDRESS SIGNAL OF DATA TO BE SELECTED
Vdata : INPUT SIGNAL VOLTAGE OF DATA TO BE SELECTED

FIG.92

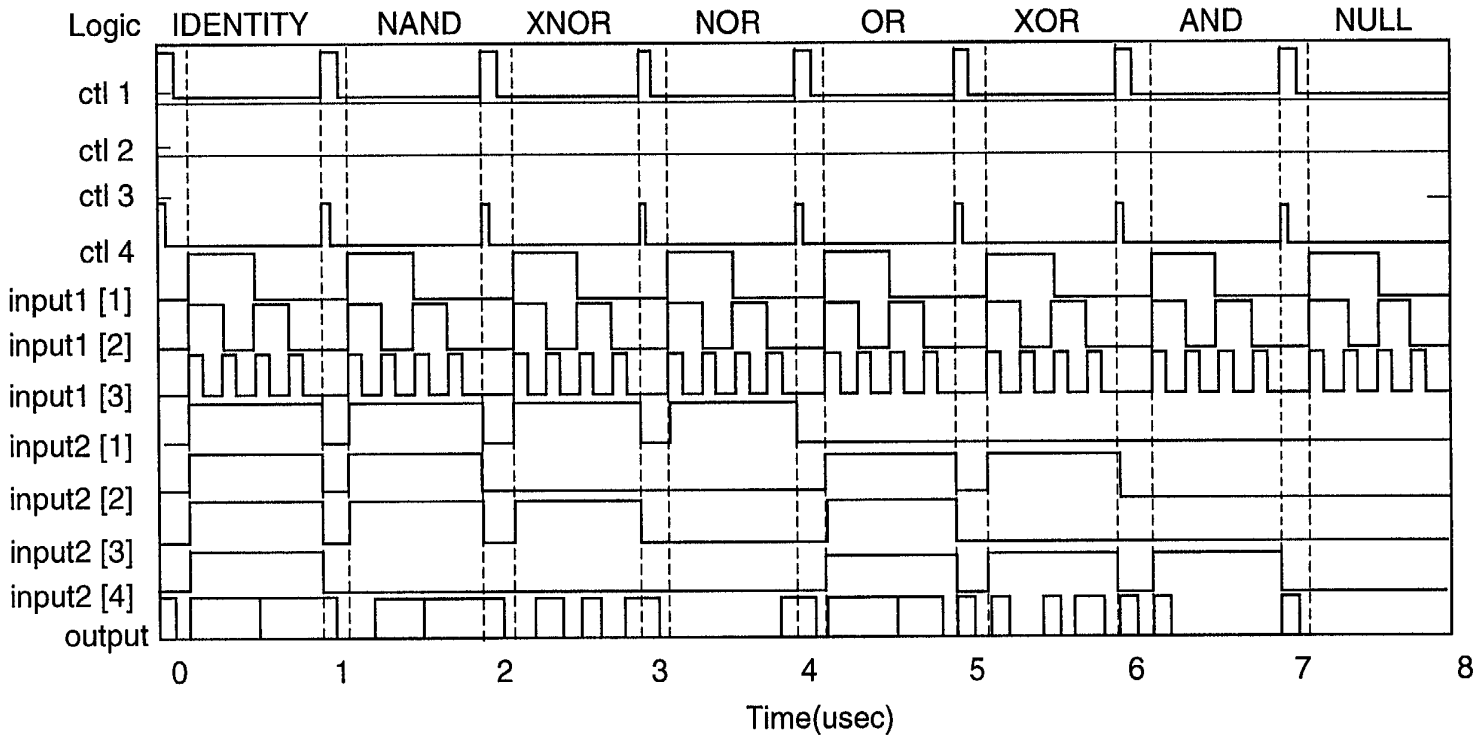


FIG.93

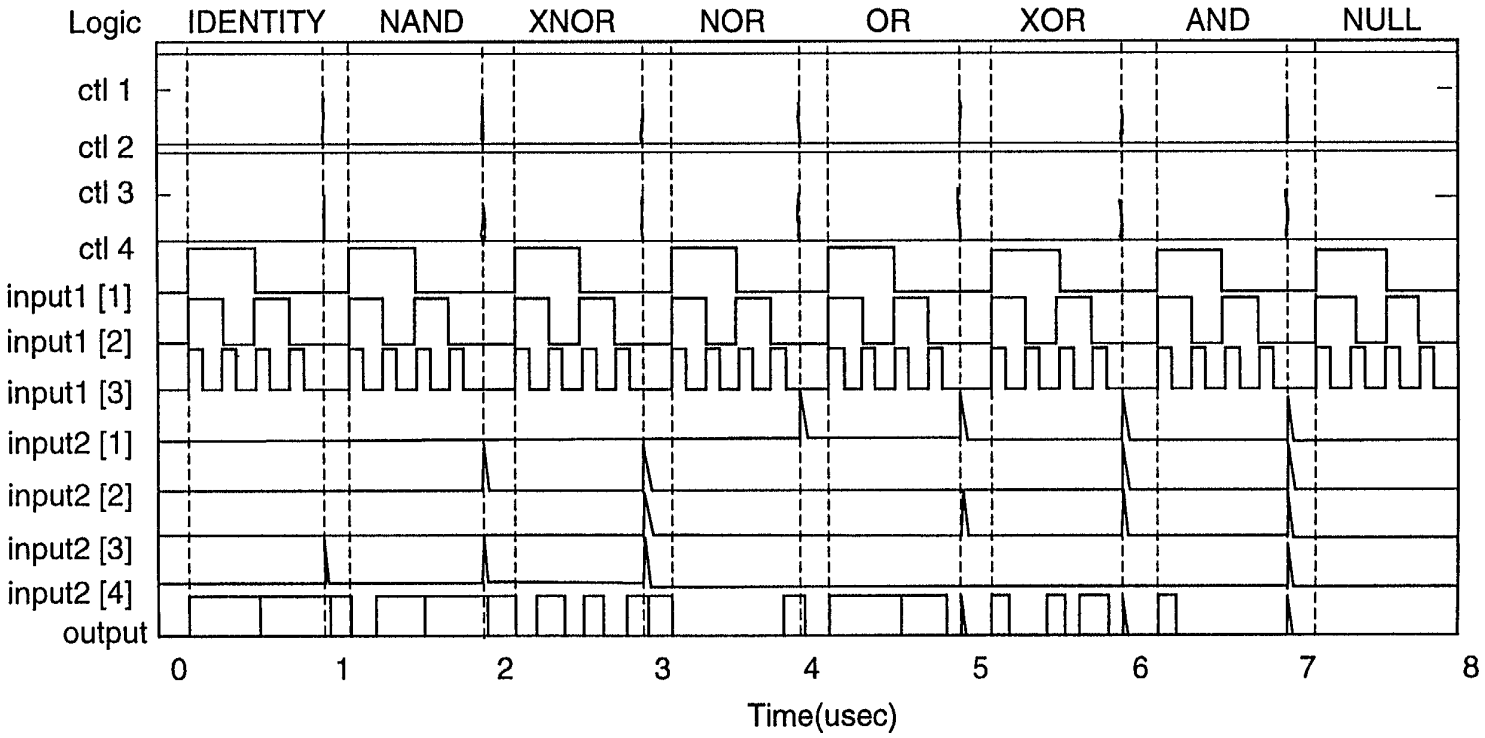


FIG.94

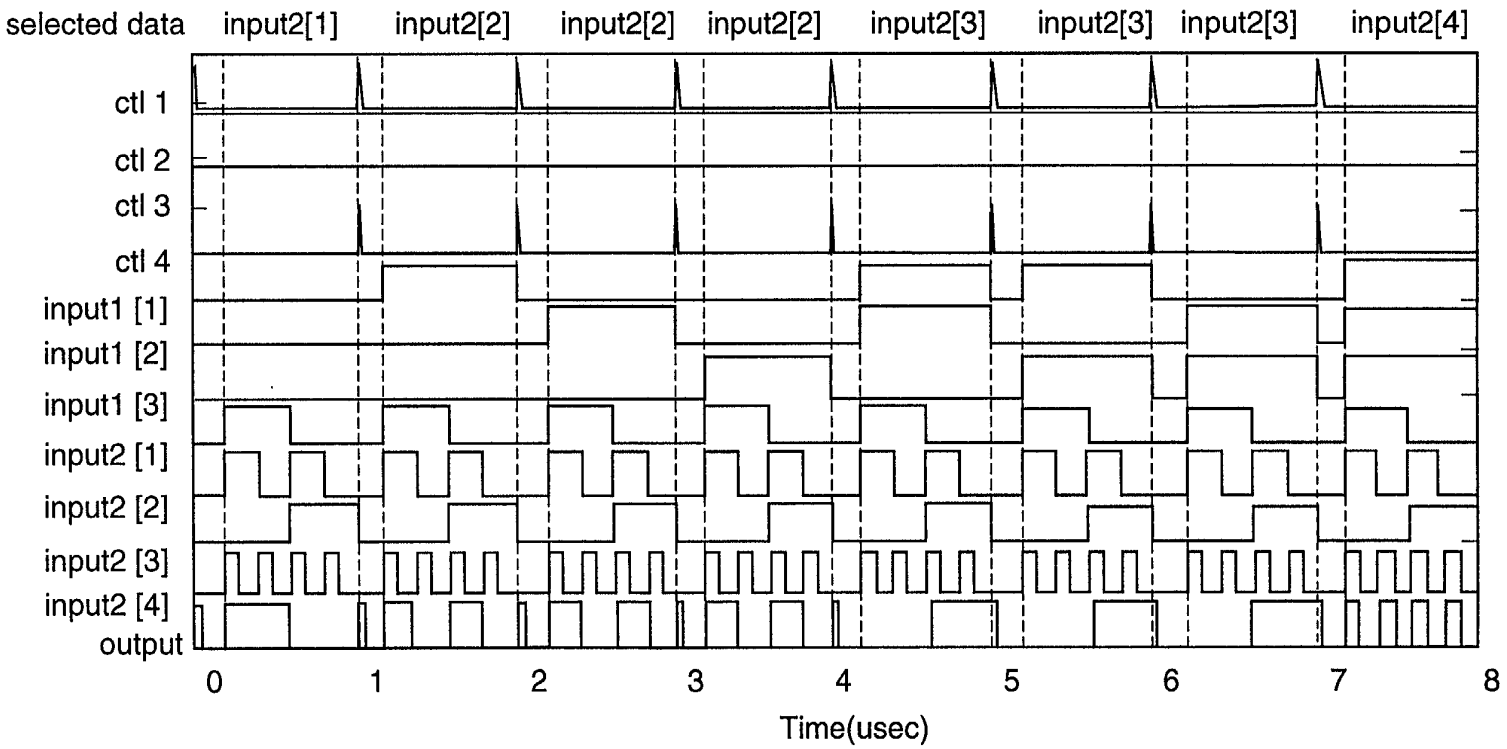

selected data
input2[1]
input2[2]
input2[2]
input2[2]
input2[3]
input2[3]
input2[3]
input2[4]
ctl 1
ctl 2
ctl 3
ctl 4
input1 [1]
input1 [2]
input1 [3]
input2 [1]
input2 [2]
input2 [3]
input2 [4]
output
0
1
2
3
4
5
6
7
8
Time(usec)

FIG.95

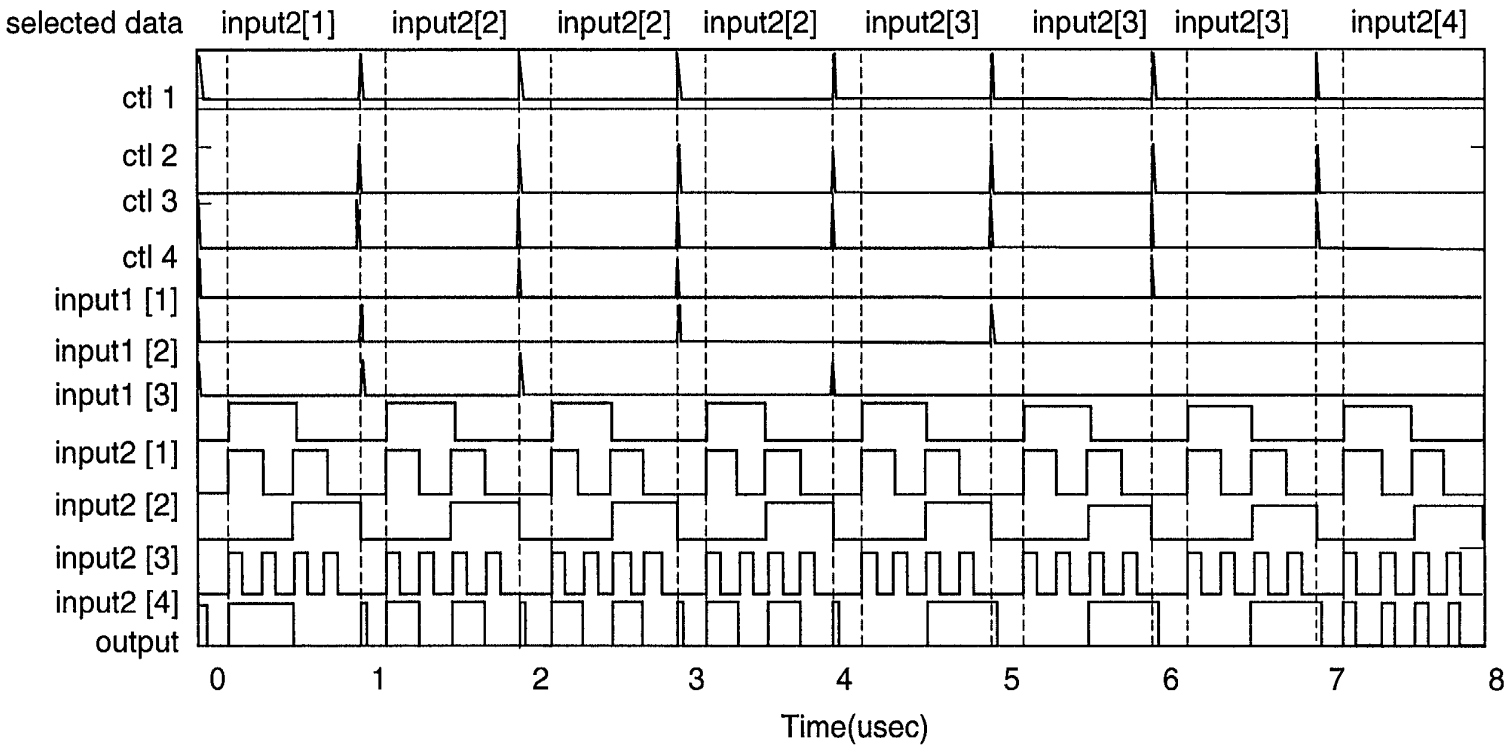

selected data
input2[1]
input2[2]
input2[2]
input2[2]
input2[3]
input2[3]
input2[3]
input2[4]
ctl 1
ctl 2
ctl 3
ctl 4
input1 [1]
input1 [2]
input1 [3]
input2 [1]
input2 [2]
input2 [3]
input2 [4]
output
0
1
2
3
4
5
6
7
8
Time(usec)

FIG.96

801 : FUNCTION RECONFIGURABLE INTEGRATED CIRCUIT

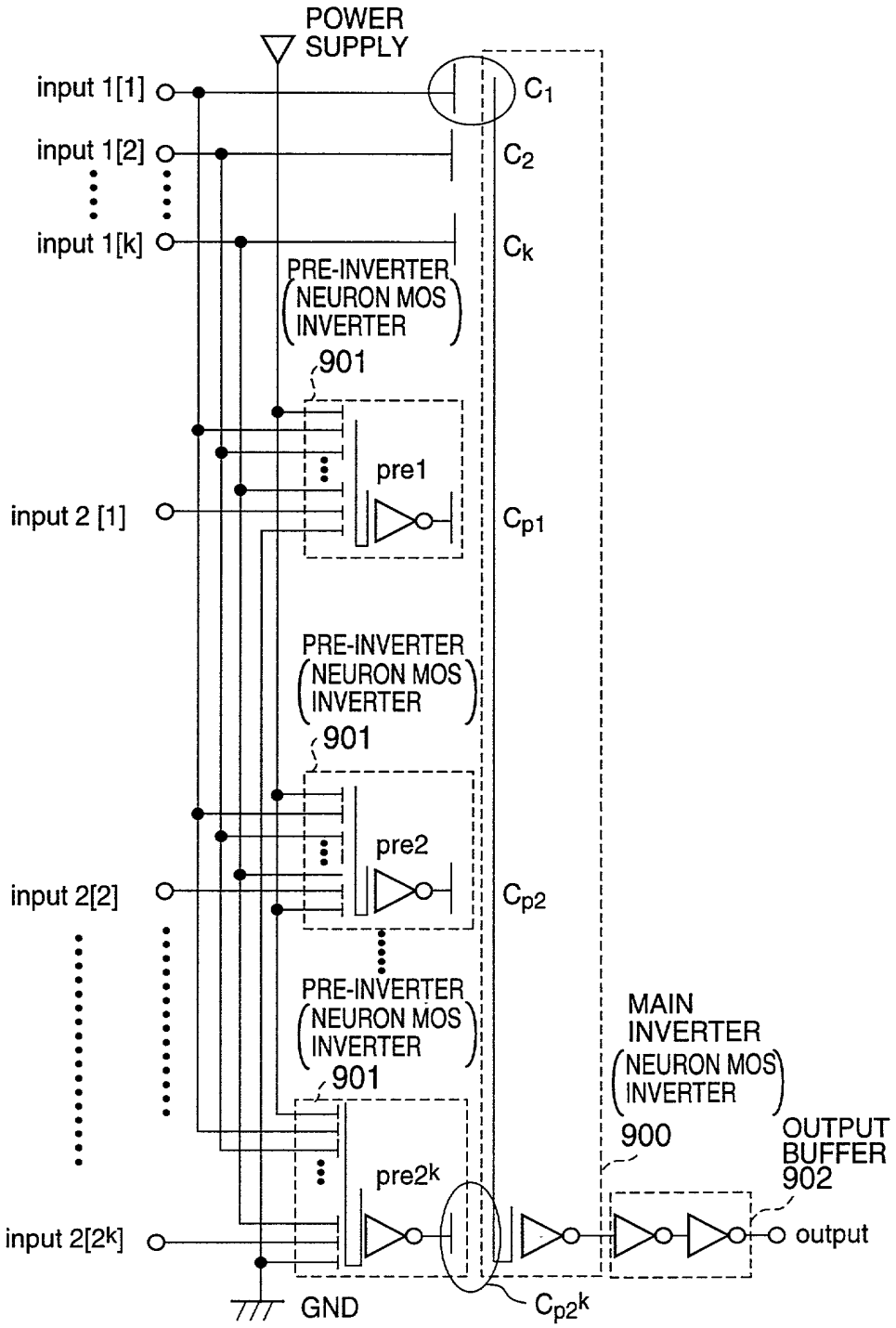


FIG.97

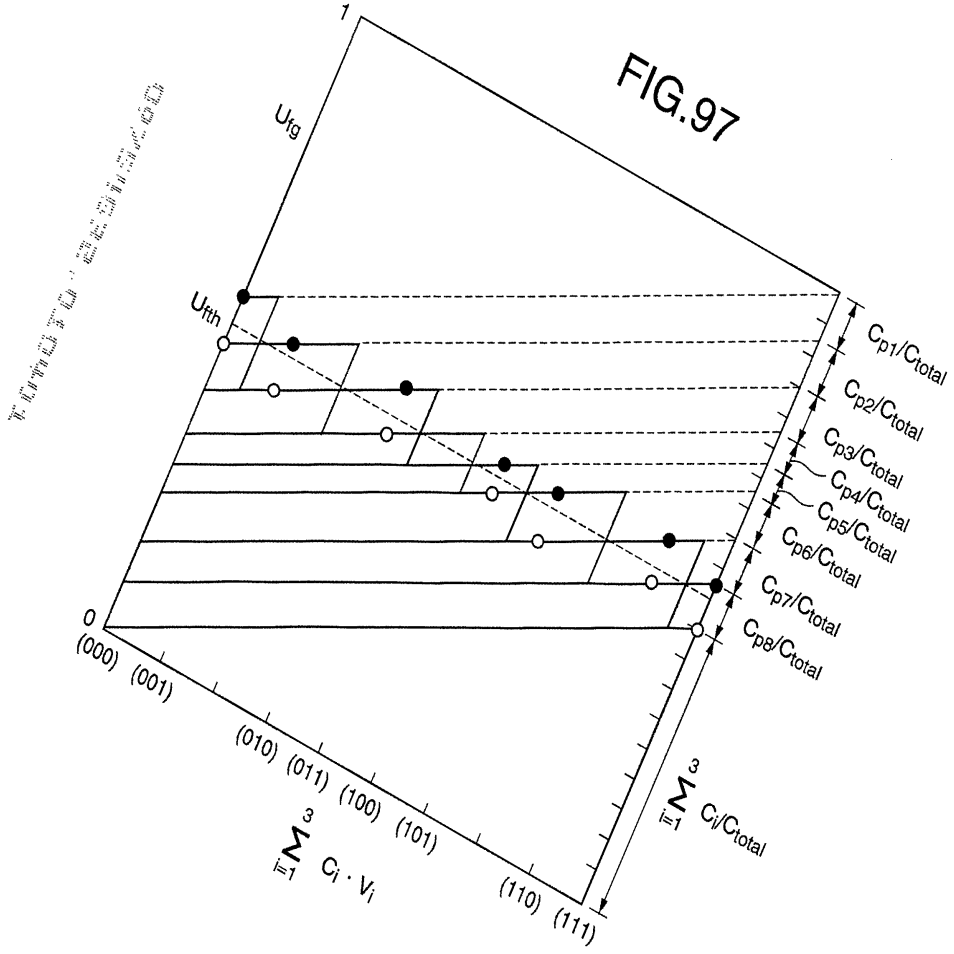

1
U_{fg}
U_{fth}
0
(000)
(001)
(010)
(011)
(100)
(101)
(110)
(111)
$\sum_{i=1}^{3} C_i \cdot V_i$
C_{p1}/C_{total}
C_{p2}/C_{total}
C_{p3}/C_{total}
C_{p4}/C_{total}
C_{p5}/C_{total}
C_{p6}/C_{total}
C_{p7}/C_{total}
C_{p8}/C_{total}
$\sum_{i=1}^{3} C_i/C_{total}$

FIG.98

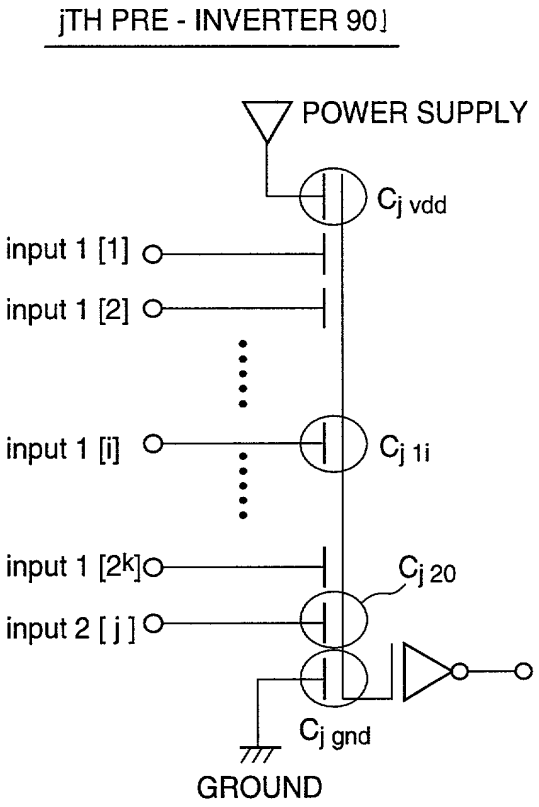

jTH PRE - INVERTER 90j
POWER SUPPLY
Cj vdd
input 1 [1]
input 1 [2]
input 1 [i]
Cj 1i
input 1 [2k]
Cj 20
input 2 [j]
Cj gnd
GROUND

FIG.99

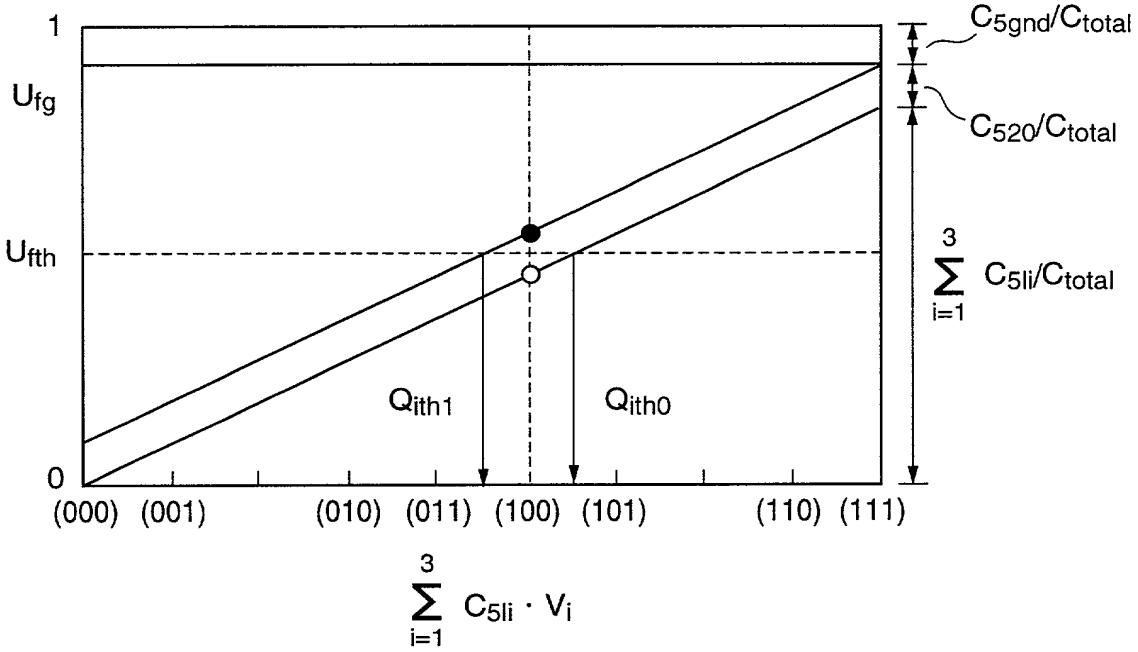

1
U_{fg}
U_{fth}
0
(000) (001) (010) (011) (100) (101) (110) (111)
Q_{ith1}
Q_{ith0}
C_{5gnd}/C_{total}
C_{520}/C_{total}
$\sum_{i=1}^{3} C_{5li}/C_{total}$
$\sum_{i=1}^{3} C_{5li} \cdot V_i$

FIG.100

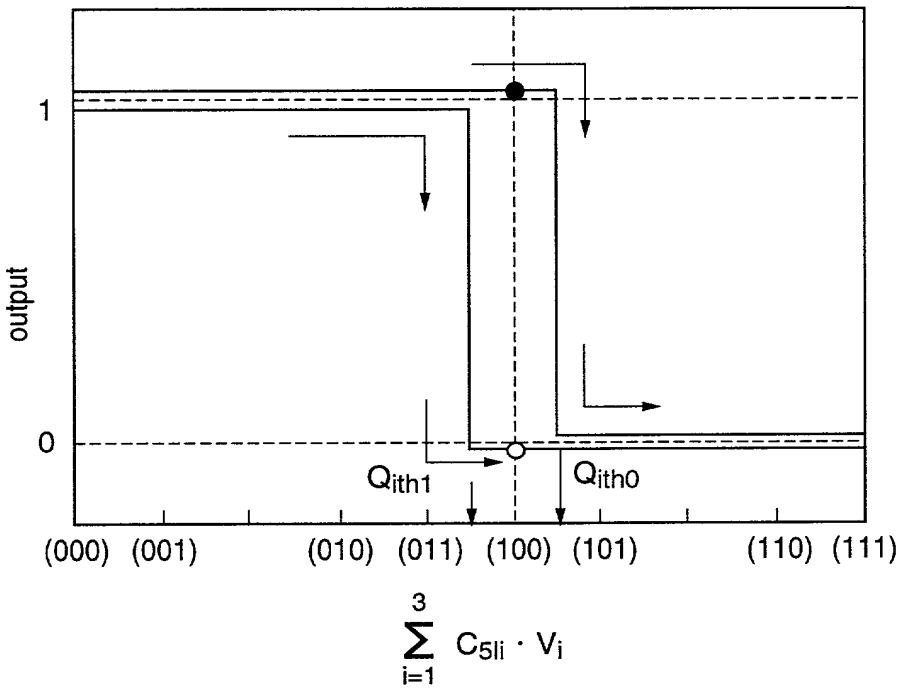

1
output
0
Q_{ith1}
Q_{ith0}
(000) (001) (010) (011) (100) (101) (110) (111)
$\sum_{i=1}^{3} C_{5li} \cdot V_i$

FIG.101A

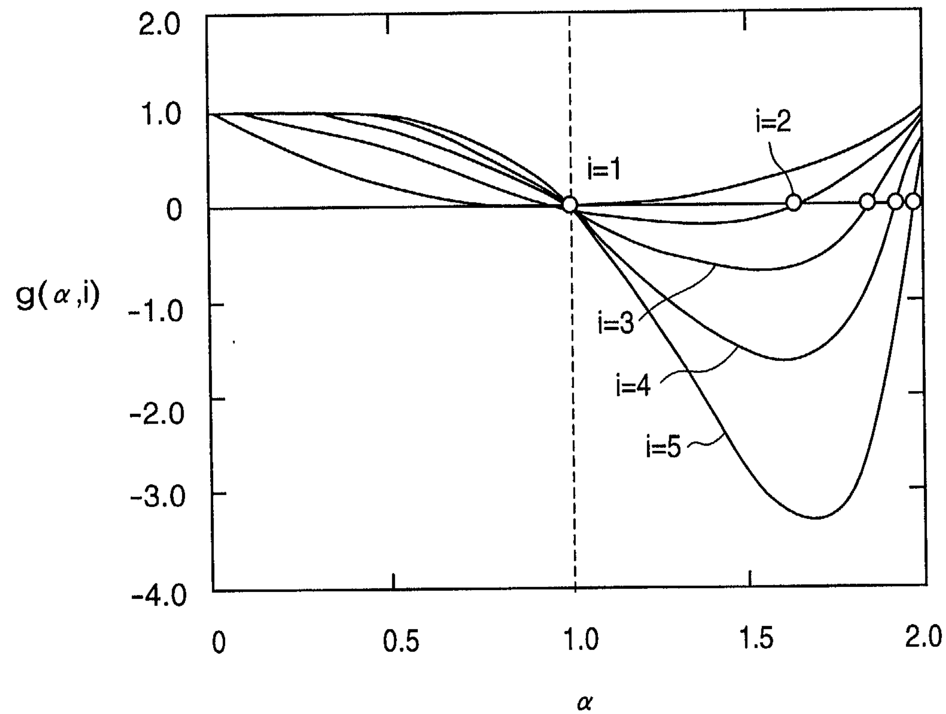


FIG.101B

i	$1.0 < \alpha < 2.0$ SOLUTION OF $g(\alpha, i)$
2	1.6180
3	1.8393
4	1.9276
5	1.9660

FIG.102

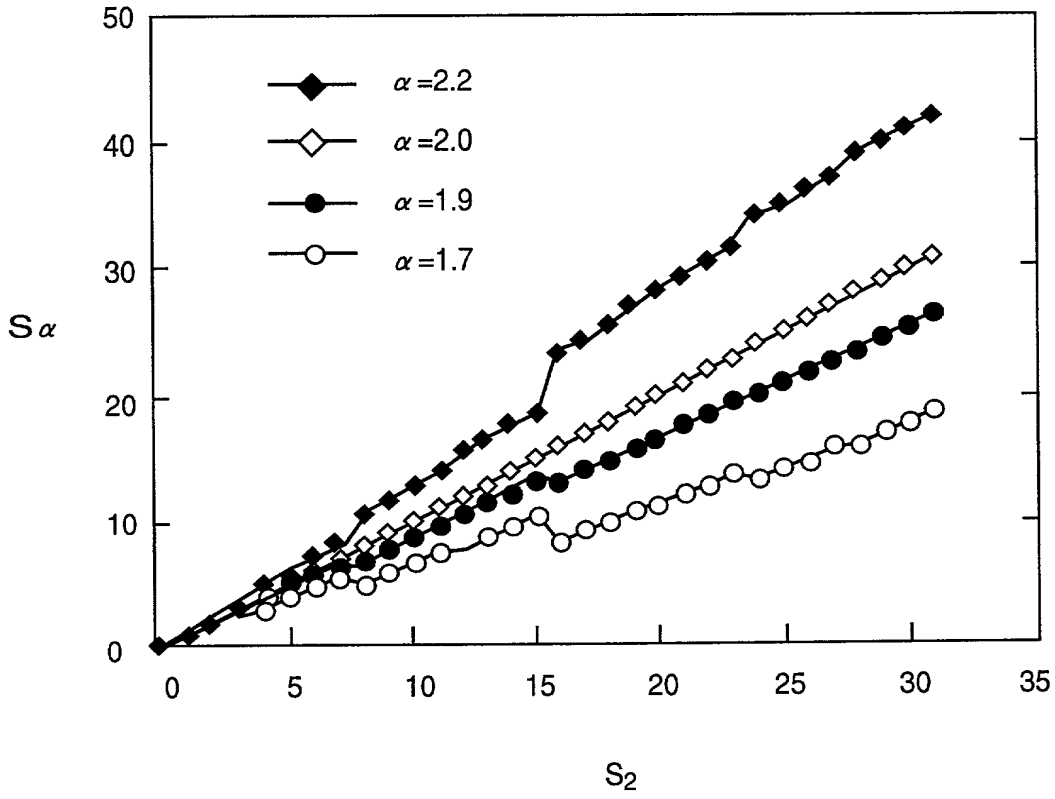


FIG.103

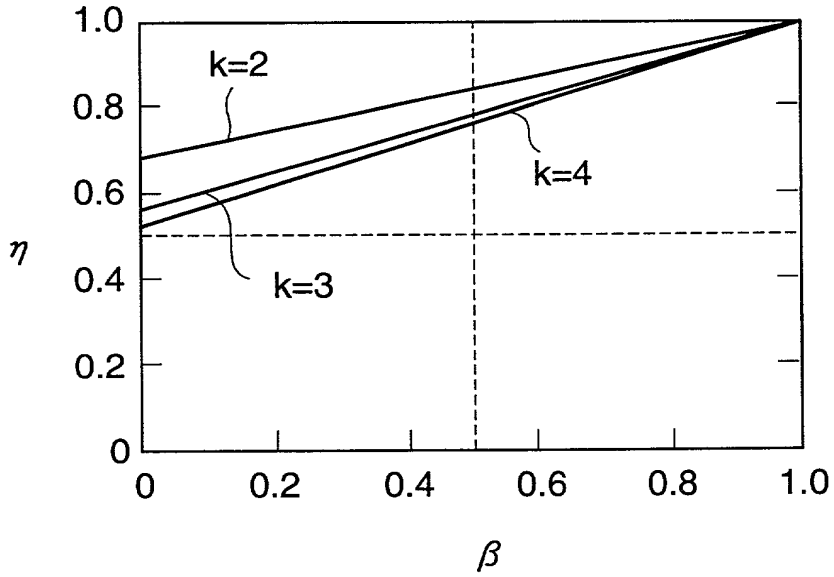


FIG.104

803 : FUNCTION RECONFIGURABLE INTEGRATED CIRCUIT

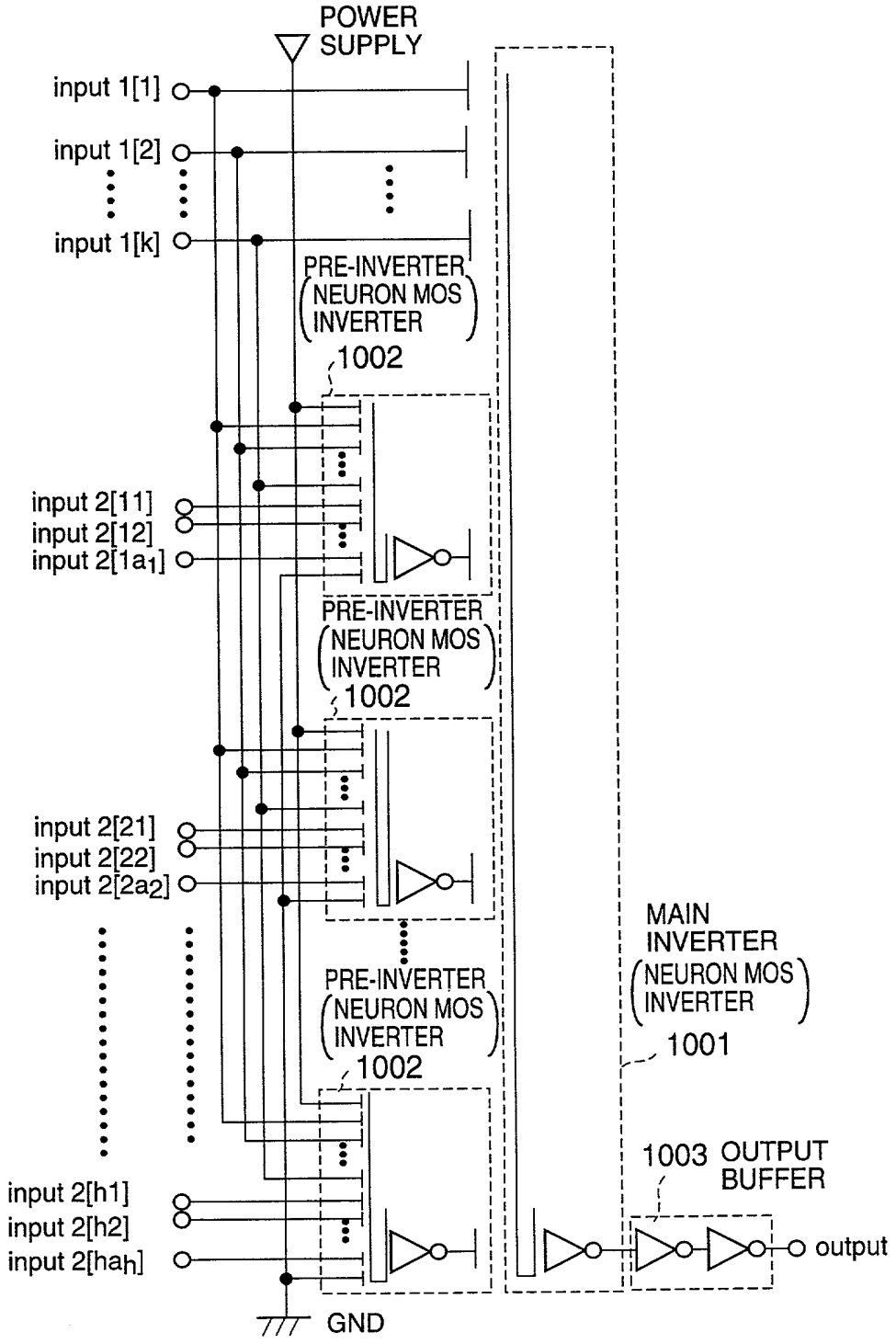


FIG.105

INV3 : NEURON MOS INVERTER

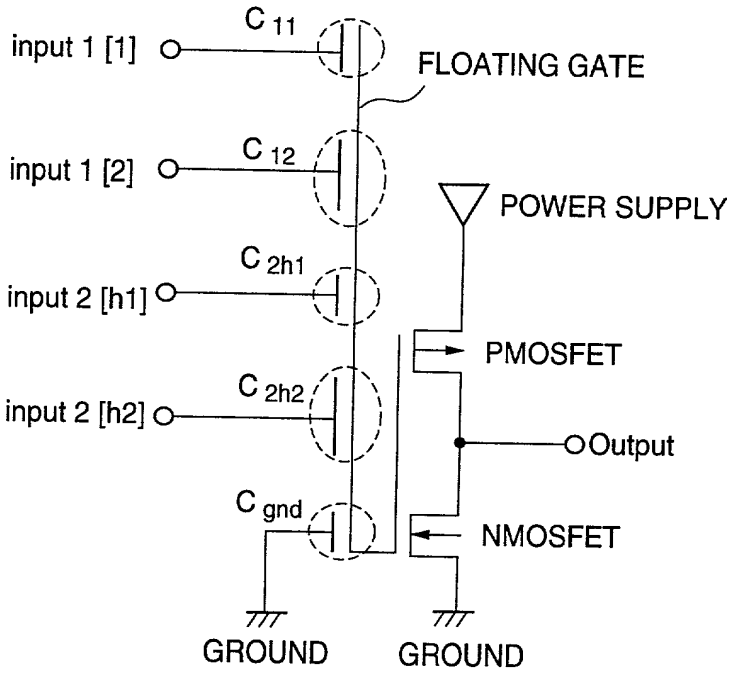


FIG.106

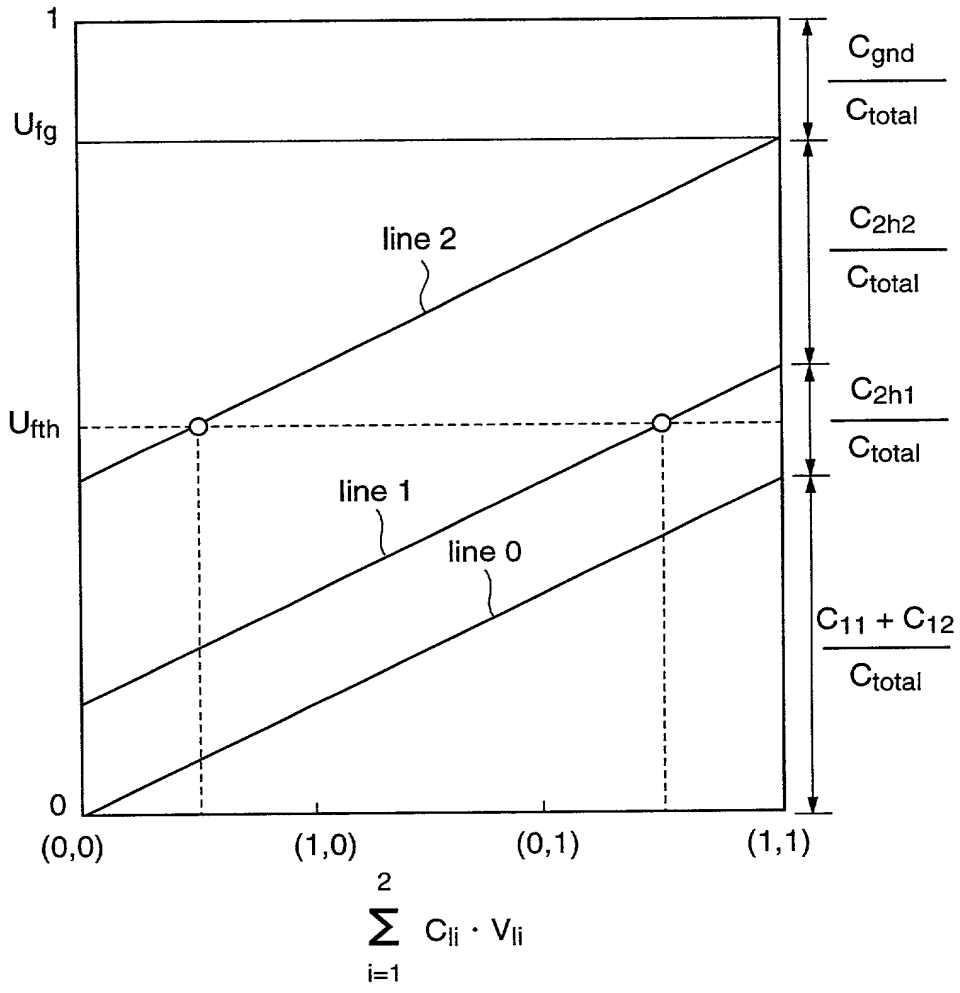

1
U_{fg}
U_{fth}
0
line 2
line 1
line 0
$\frac{C_{gnd}}{C_{total}}$
$\frac{C_{2h2}}{C_{total}}$
$\frac{C_{2h1}}{C_{total}}$
$\frac{C_{11} + C_{12}}{C_{total}}$
(0,0)
(1,0)
(0,1)
(1,1)
$\sum_{i=1}^{2} C_{li} \cdot V_{li}$

FIG.107

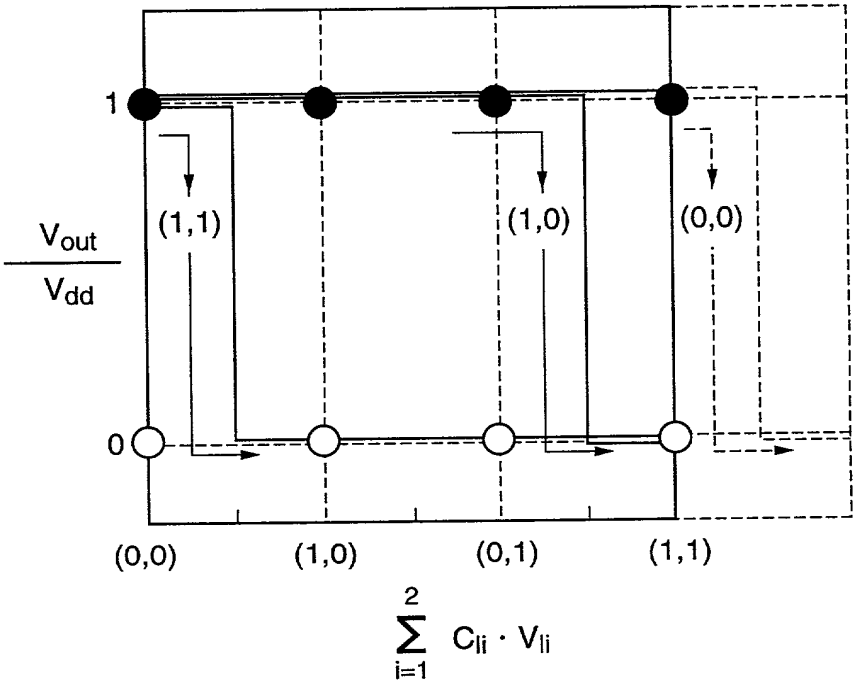


FIG.108

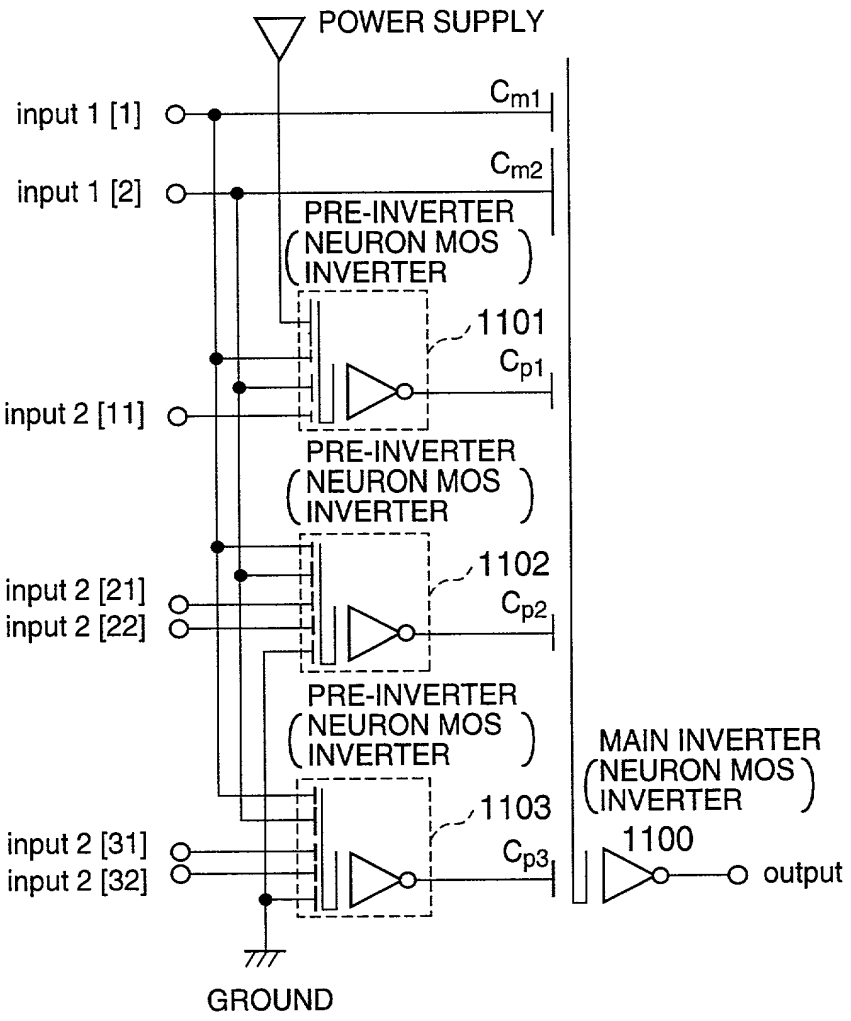

POWER SUPPLY
input 1 [1]
input 1 [2]
C_{m1}
C_{m2}
PRE-INVERTER (NEURON MOS INVERTER)
1101
C_{p1}
input 2 [11]
PRE-INVERTER (NEURON MOS INVERTER)
1102
C_{p2}
input 2 [21]
input 2 [22]
PRE-INVERTER (NEURON MOS INVERTER)
MAIN INVERTER (NEURON MOS INVERTER)
1103
1100
C_{p3}
input 2 [31]
input 2 [32]
output
GROUND

FIG.109

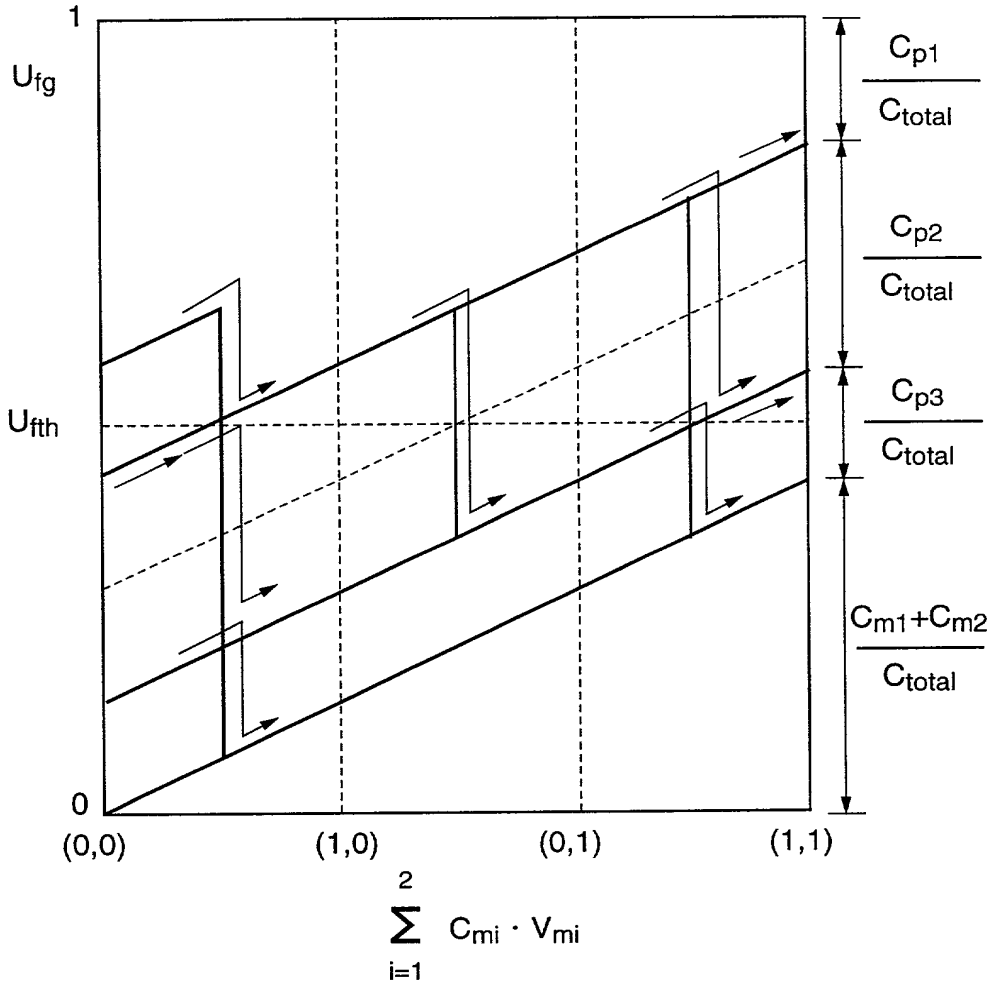

1
U_{fg}
U_{fth}
0
(0,0)
(1,0)
(0,1)
(1,1)
$\frac{C_{p1}}{C_{total}}$
$\frac{C_{p2}}{C_{total}}$
$\frac{C_{p3}}{C_{total}}$
$\frac{C_{m1}+C_{m2}}{C_{total}}$
$\sum_{i=1}^{2} C_{mi} \cdot V_{mi}$

FIG.110

INPUT VARIABLE (X_1,X_2)	$U_{fg}(Y_{p2},Y_{p3})$							
	#0 (NULL)	#1 (AND)	#2	#3	#4	#5	#6 (XOR)	#7 (OR)
(0,0)	0(1,1)	0(1,1)	0(1,1)	0(1,1)	0(1,1)	0(1,1)	0(1,1)	0(1,1)
(1,0)	0(0,0)	0(0,1)	0(1,0)	0(1,0)	1(1,1)	1(1,1)	1(1,1)	1(1,1)
(0,1)	0(0,0)	0(0,1)	1(1,0)	1(1,0)	0(0,1)	0(0,1)	1(1,1)	1(1,1)
(1,1)	0(0,0)	1(0,1)	0(0,0)	1(1,0)	0(0,0)	1(0,1)	0(0,0)	1(1,1)

FIG.111

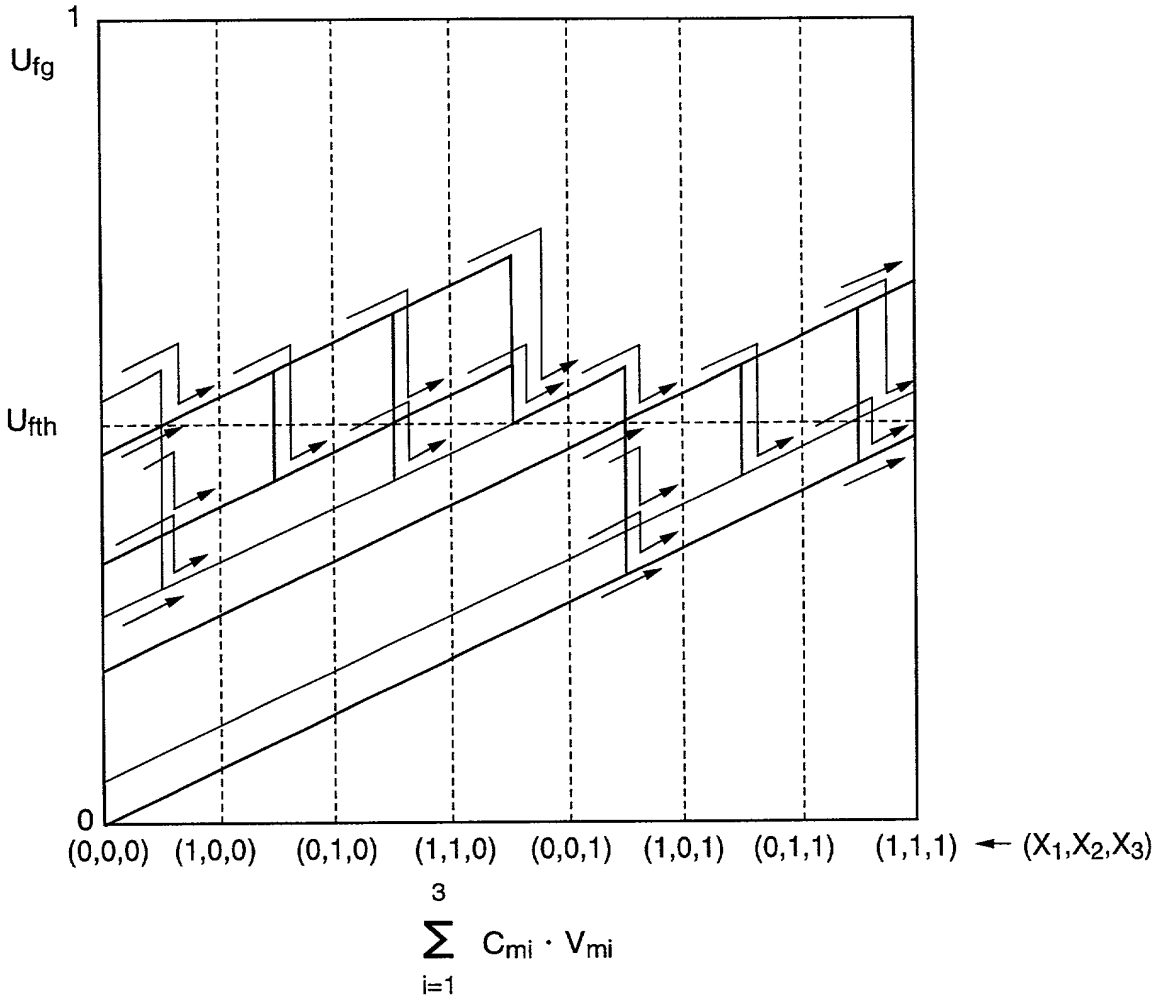

1
U_{fg}
U_{fth}
0
(0,0,0)
(1,0,0)
(0,1,0)
(1,1,0)
(0,0,1)
(1,0,1)
(0,1,1)
(1,1,1)
(X_1,X_2,X_3)
$\sum_{i=1}^{3} C_{mi} \cdot V_{mi}$

FIG.112

805 : FUNCTION RECONFIGURABLE INTEGRATED CIRCUIT

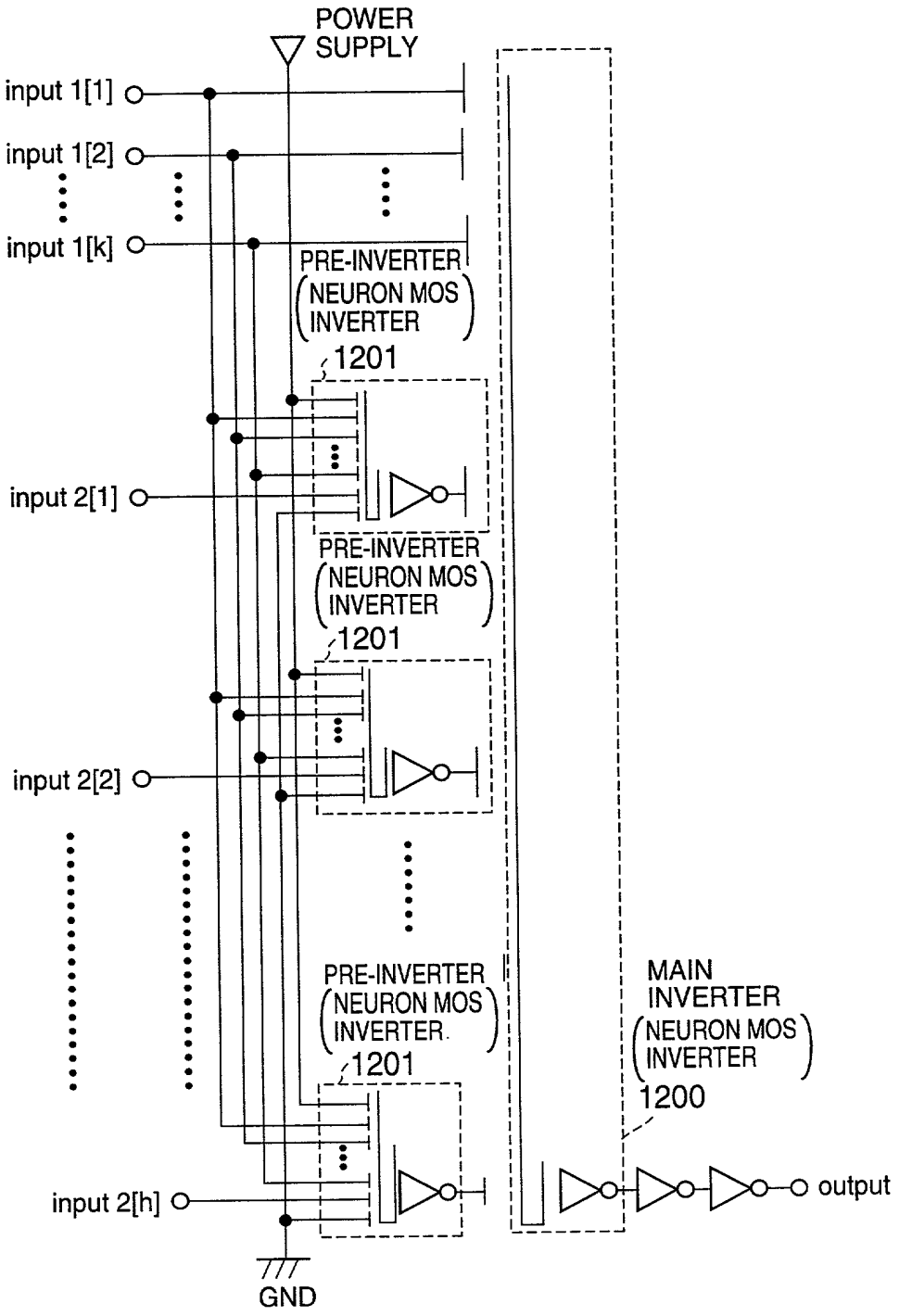


FIG.113

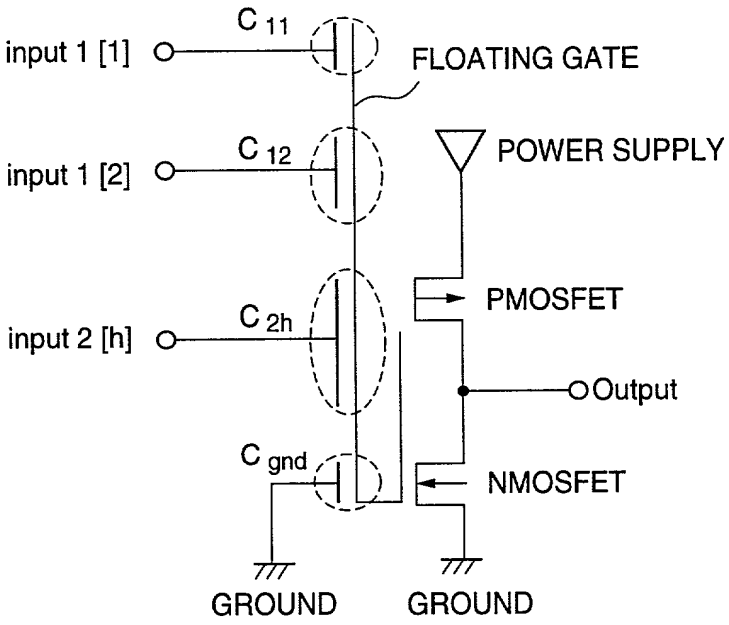

C 11
input 1 [1]
FLOATING GATE
C 12
input 1 [2]
POWER SUPPLY
PMOSFET
C 2h
input 2 [h]
Output
C gnd
NMOSFET
GROUND
GROUND

FIG.114

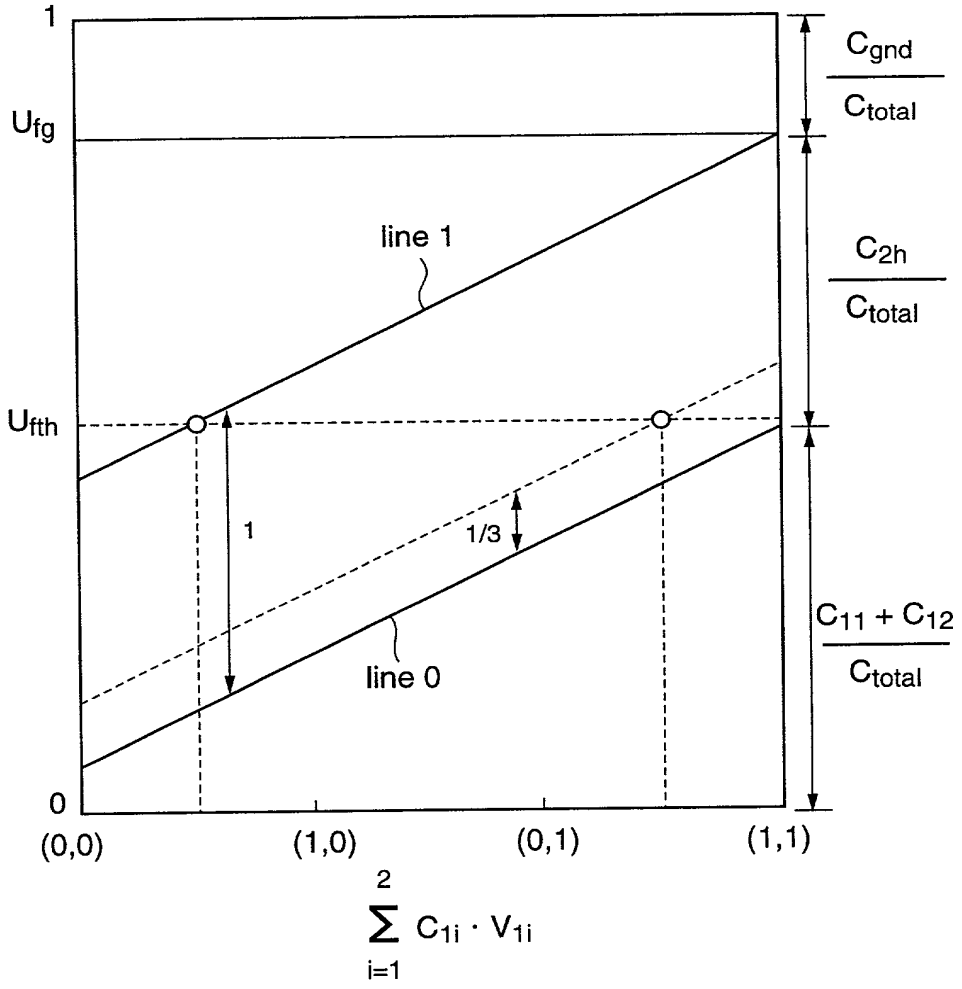
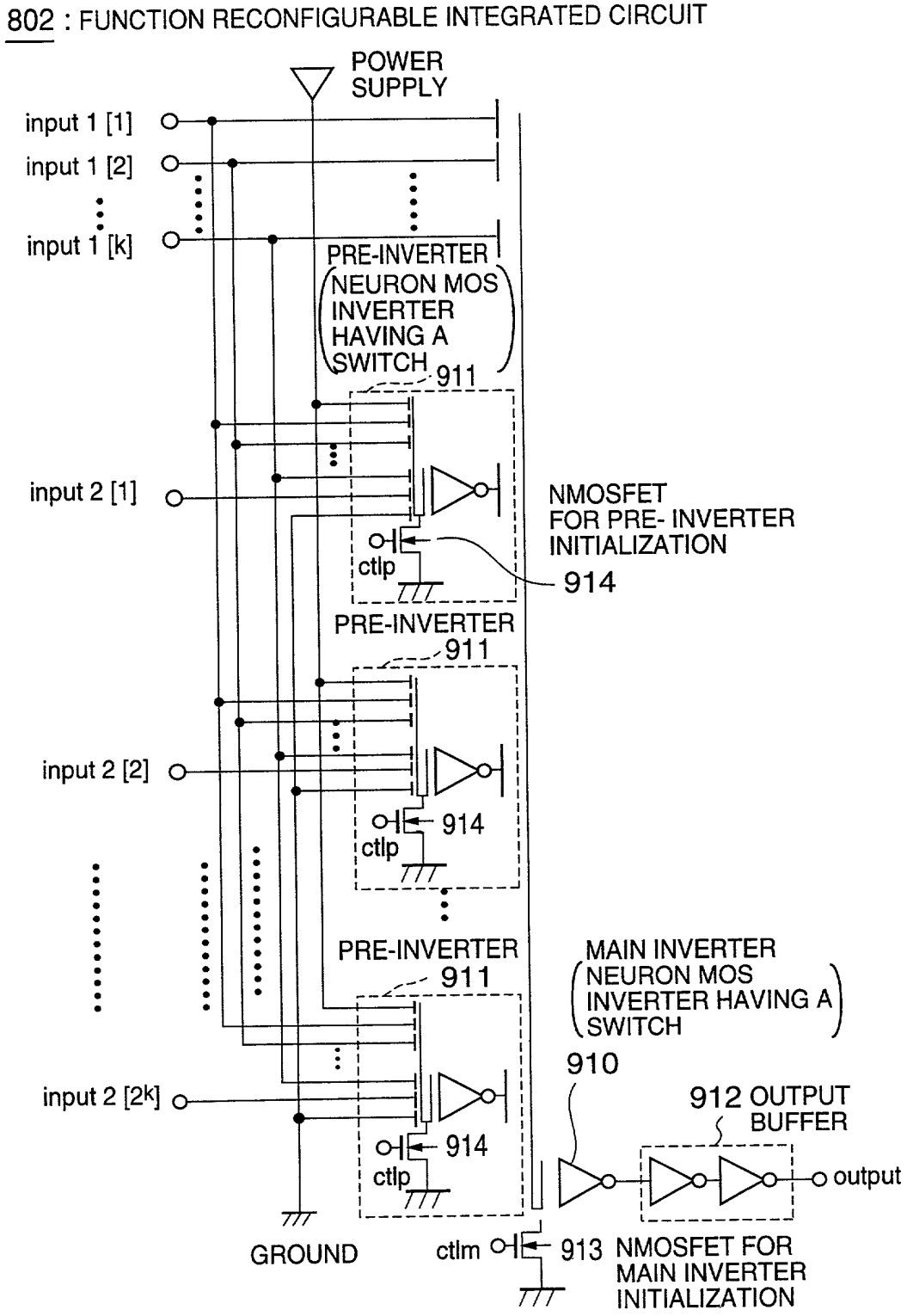

1
U_{fg}
U_{fth}
0
line 1
line 0
1
1/3
(0,0)
(1,0)
(0,1)
(1,1)
$\frac{C_{gnd}}{C_{total}}$
$\frac{C_{2h}}{C_{total}}$
$\frac{C_{11} + C_{12}}{C_{total}}$
$\sum_{i=1}^{2} C_{1i} \cdot V_{1i}$

FIG.115


802 : FUNCTION RECONFIGURABLE INTEGRATED CIRCUIT
POWER SUPPLY
input 1 [1]
input 1 [2]
input 1 [k]
PRE-INVERTER (NEURON MOS INVERTER HAVING A SWITCH
911
input 2 [1]
NMOSFET FOR PRE- INVERTER INITIALIZATION
914
ctlp
PRE-INVERTER
911
input 2 [2]
914
ctlp
PRE-INVERTER
911
MAIN INVERTER (NEURON MOS INVERTER HAVING A SWITCH
910
input 2 [2k]
912 OUTPUT BUFFER
914
ctlp
output
GROUND
ctlm
913 NMOSFET FOR MAIN INVERTER INITIALIZATION